

Improving Error-Resilience of Emerging Multi-Value Technologies

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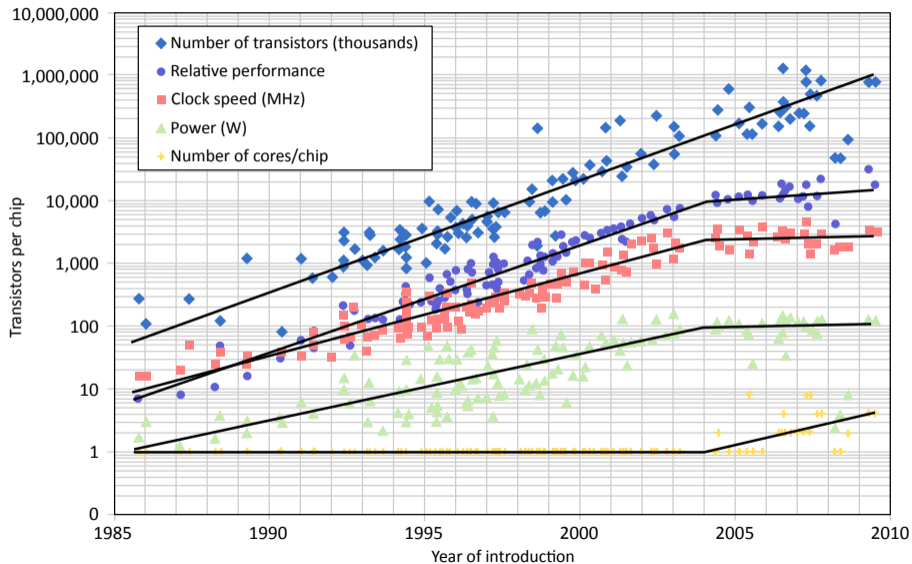
Jan 20, 2016



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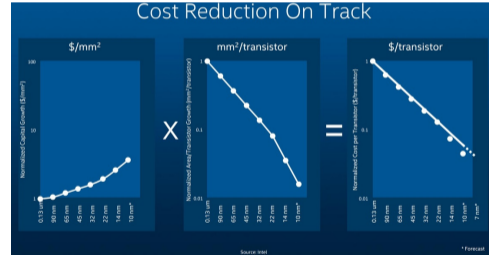
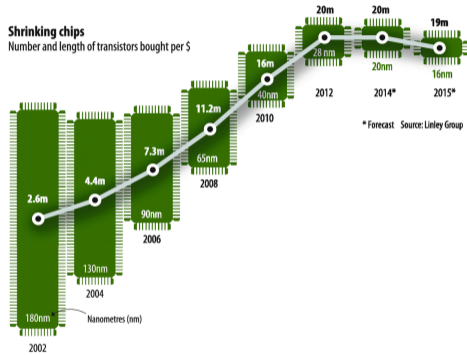


Moore's Law Struggling with CMOS



¹ National Research Council, "The Future of Computing Performance: Game Over or Next Level?", 2011.

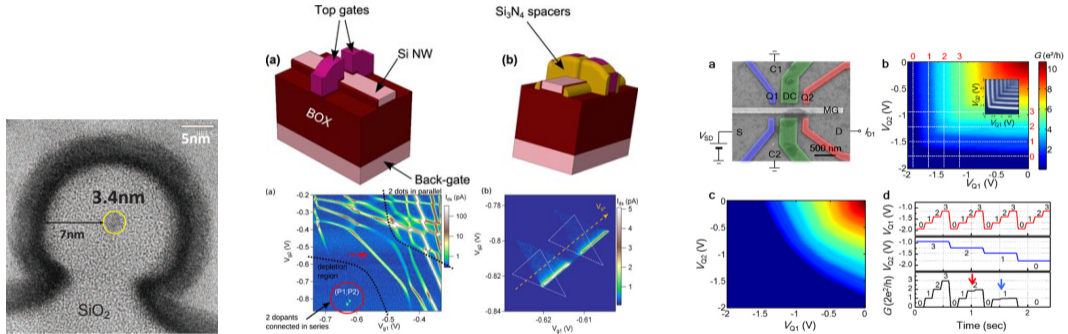
Moore's Law



¹ The economist, "A golden rule of microchips appears to be coming to an end", Nov. 18, 2013.

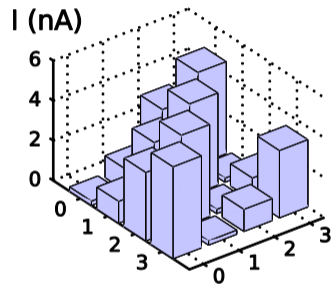
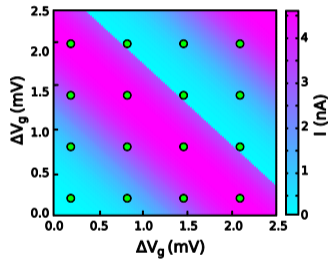
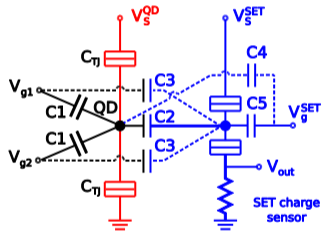
² Vivek Singh, Intel, "Moore's Law at 50: No End in Sight", DAC 2015 keynote.

Emerging Technologies to the Rescue?



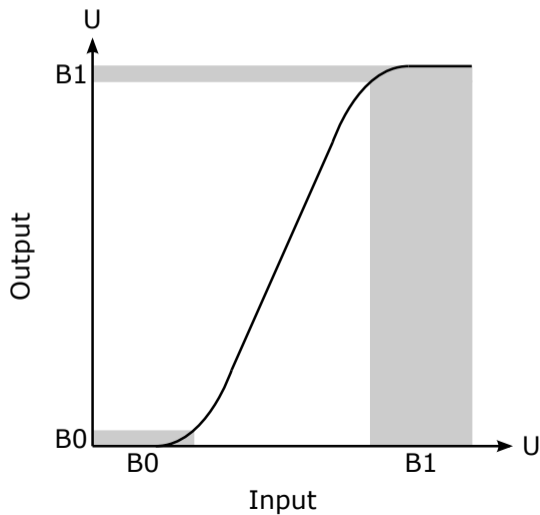
- 1 R. Lavieville et al., "350K Operating Silicon Nanowire Single Electron/Hole Transistors Scaled Down to 3.4nm Diameter and 10nm Gate Length" EUROSOI-ULIS, Jan., 2015.
- 2 X. Jehl et al., "The coupled atom transistor" Journal of Physics: Condensed Matter, 2015.
- 3 M. Seo et al., "Multi-valued logic gates based on ballistic transport in quantum point contacts" Scientific Reports, 4, 2014.

Quantum Dot SET Half Adder

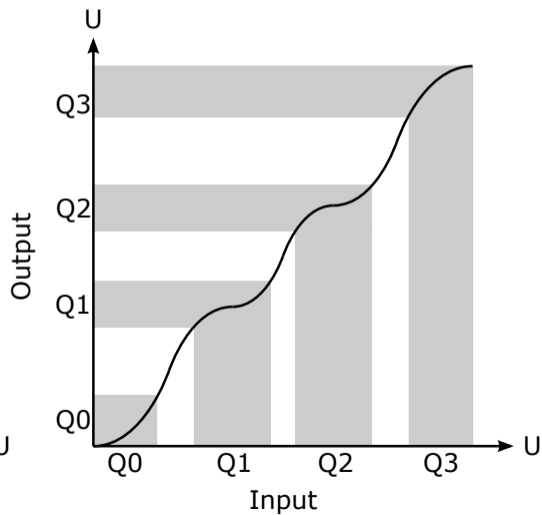


Multi-Valued Logic

Binary

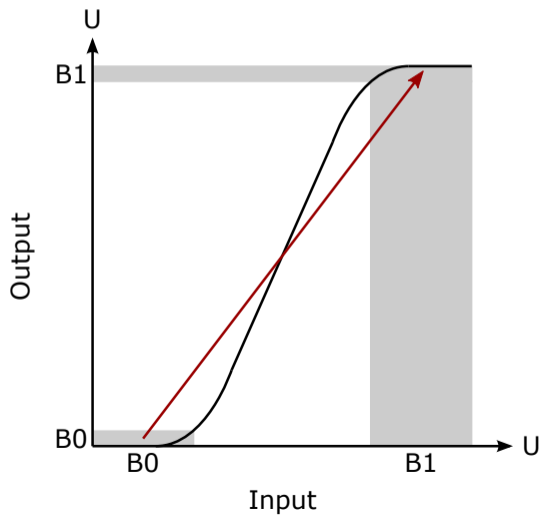


Quaternary

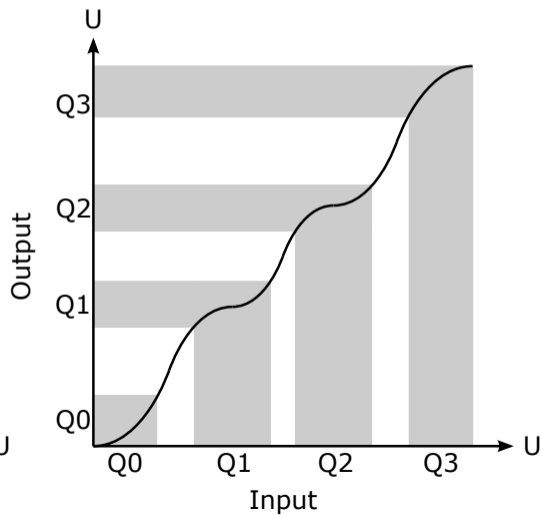


Multi-Valued Logic

Binary

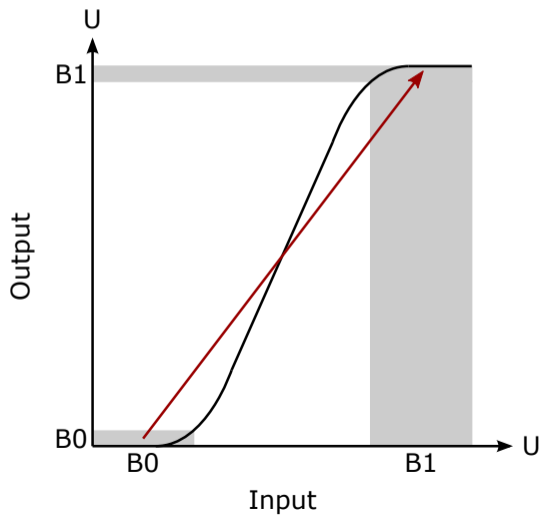


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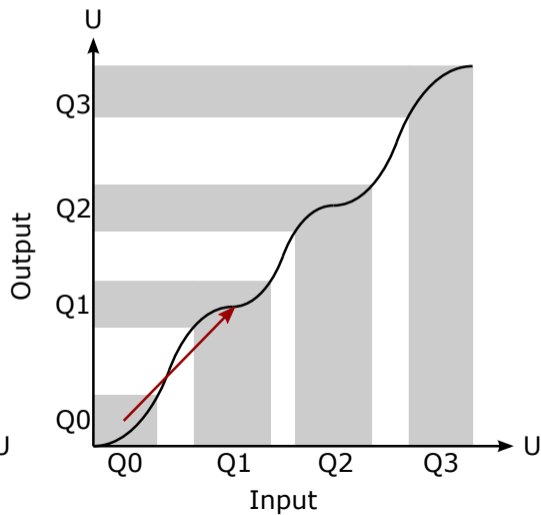


Multi-Valued Logic

Binary

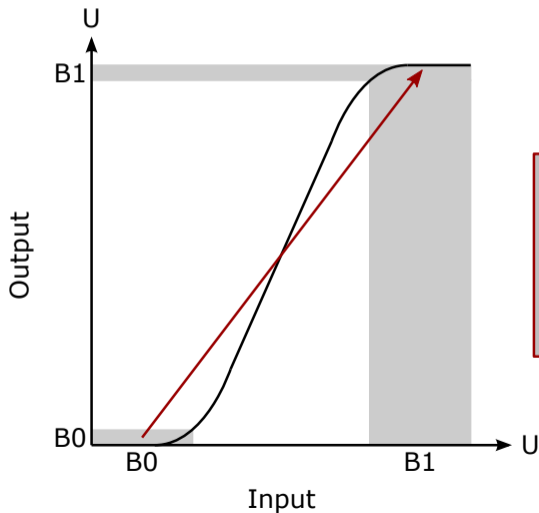


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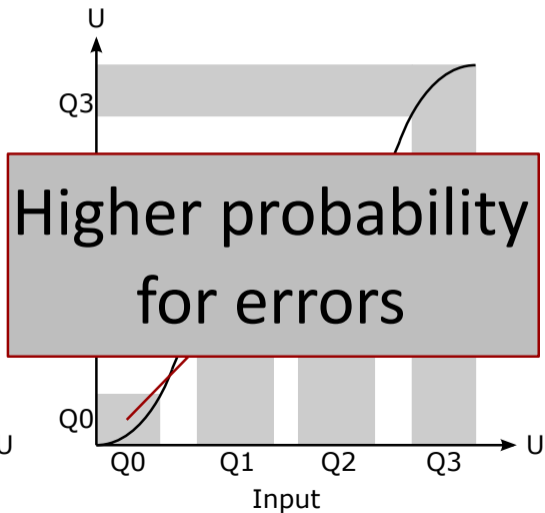


Multi-Valued Logic

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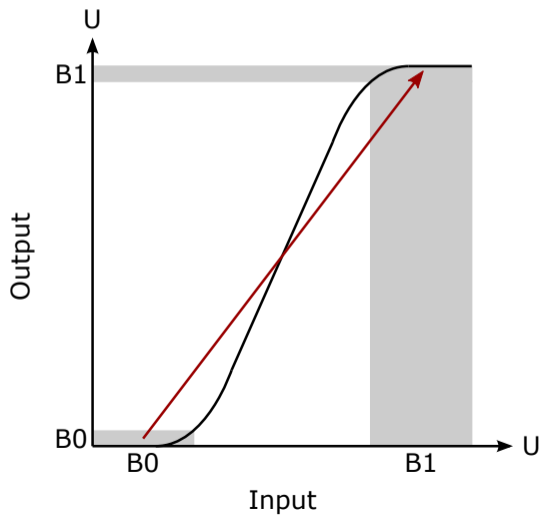


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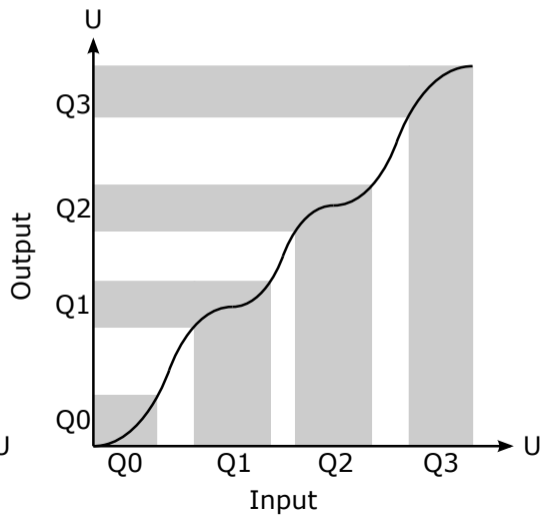


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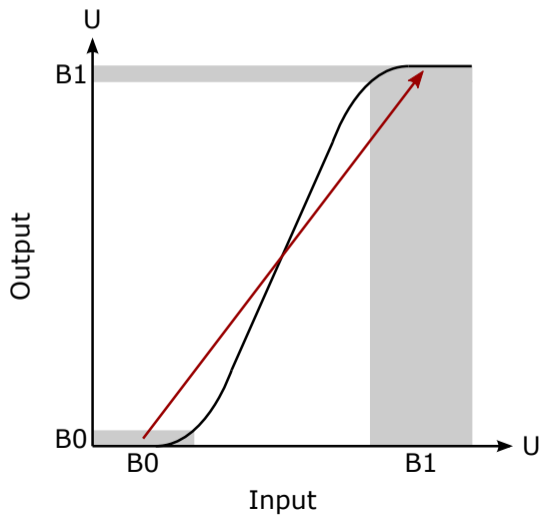


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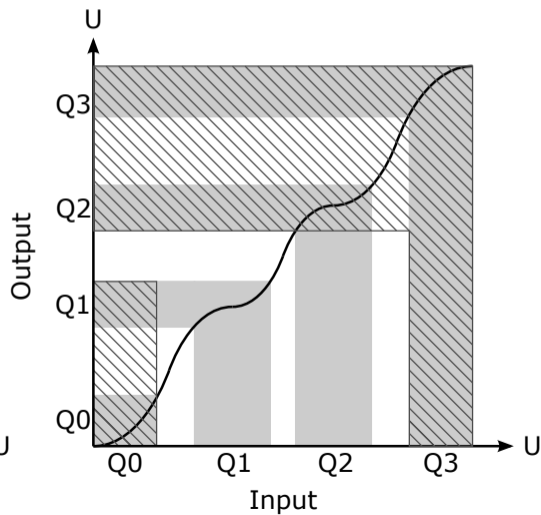


Multi-Valued Logic

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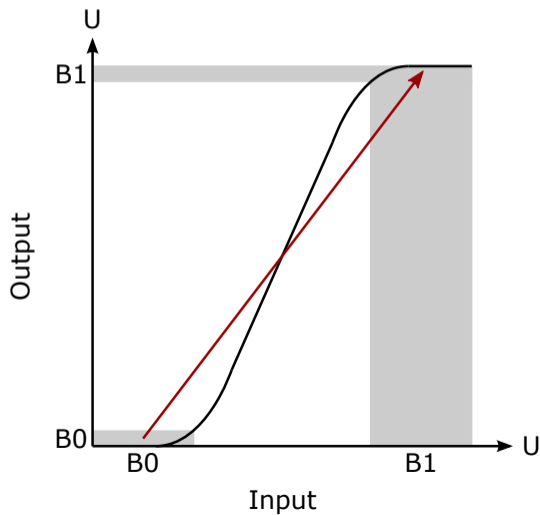


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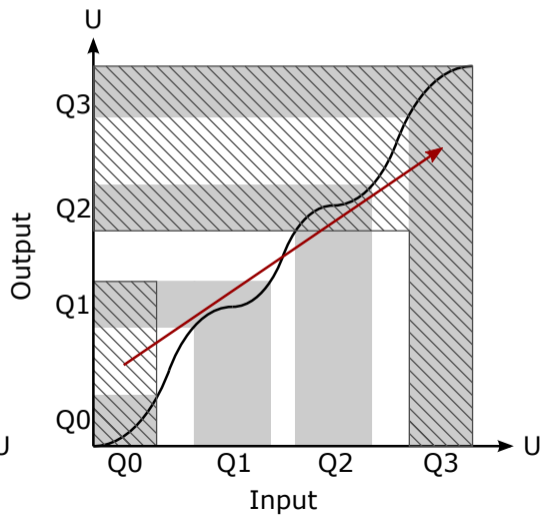


Multi-Valued Logic

Binary

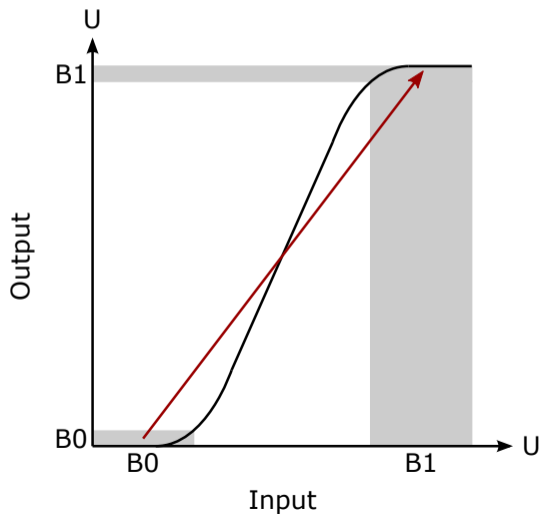


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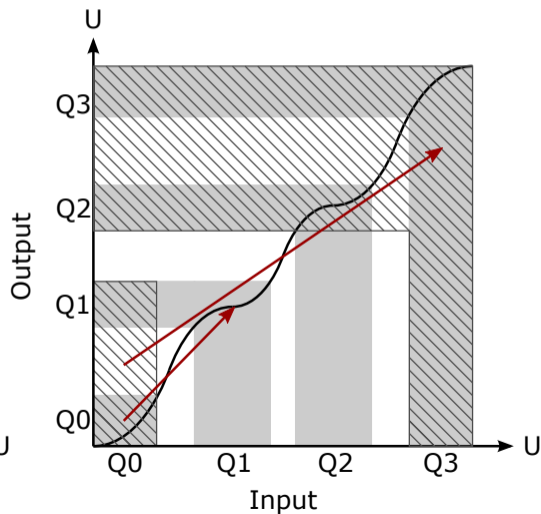


Multi-Valued Logic

Binary



Quaternary



Multi-Valued Logic

Binary



Quaternary

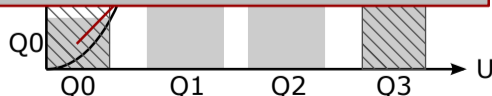


Treat data differently

- Binary for increased noise tolerance
- Quaternary for increased entropy



Input



Input

Dual-Mode Gates

OR

B \ A	0	1	2	3
0	0	1	2	3
1	1	1	3	3
2	2	3	2	3
3	3	3	3	3

AND

B \ A	0	1	2	3
0	0	0	0	0
1	0	1	0	1
2	0	0	2	2
3	0	1	2	3

XOR

B \ A	0	1	2	3
0	0	1	2	3
1	1	0	3	2
2	2	3	0	1
3	3	2	1	0

MAX

B \ A	0	1	2	3
0	0	1	2	3
1	1	1	2	3
2	2	2	2	3
3	3	3	3	3

MIN

B \ A	0	1	2	3
0	0	0	0	0
1	0	1	1	1
2	0	1	2	2
3	0	1	2	3

INV

A	\bar{A}
0	3
1	2
2	1
3	0

Dual-Mode Adder?

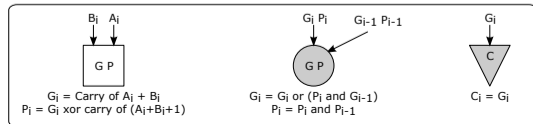
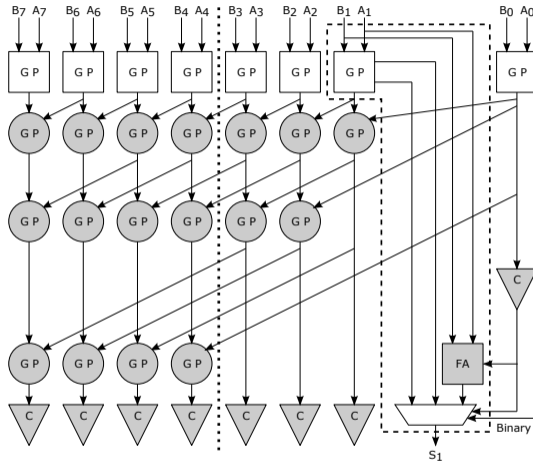
HA

B \ A	0	1	2	3
0	0	1	2	3
1	1	2	3	0
2	2	3	0	1
3	3	0	1	2

FA (carry=1)

B \ A	0	1	2	3
0	1	2	3	0
1	2	3	0	1
2	3	0	1	2
3	0	1	2	3

Carry-Lookahead Adder



Dual-Mode Adder

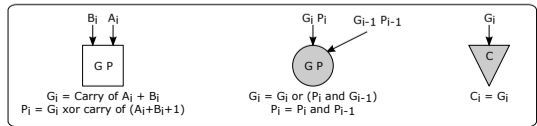
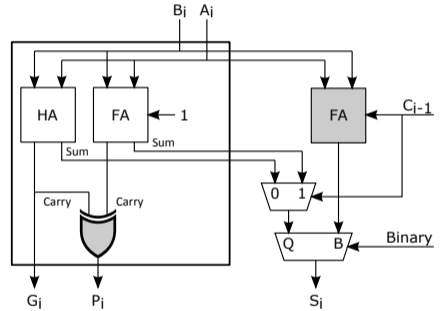
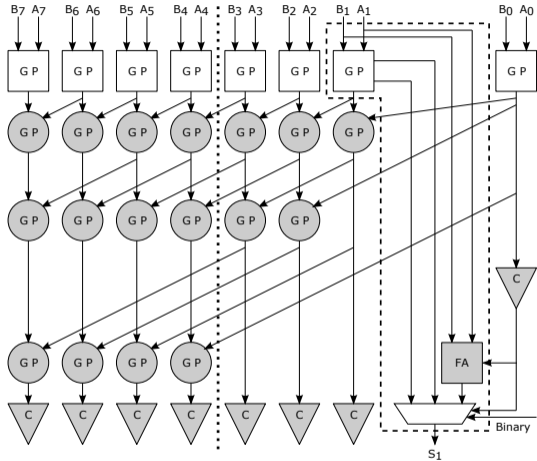
HA

B \ A	0	1	2	3
0	0	0	0	0
1	0	0	0	1
2	0	0	1	1
3	0	1	1	1

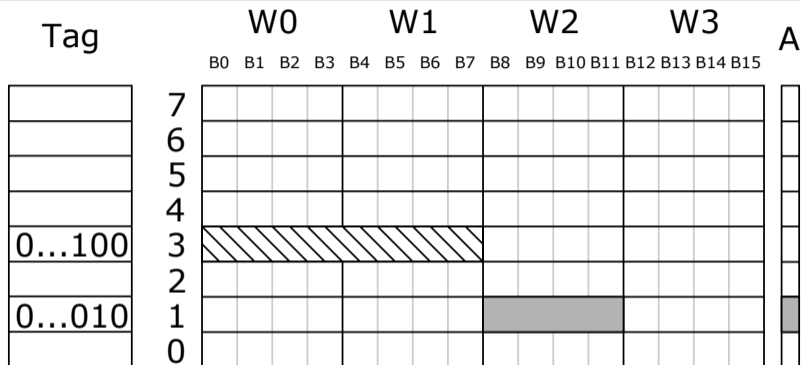
FA (carry=1)

B \ A	0	1	2	3
0	0	0	0	1
1	0	0	1	1
2	0	1	1	1
3	1	1	1	1

Carry-Lookahead Adder



Dual-Mode Caches



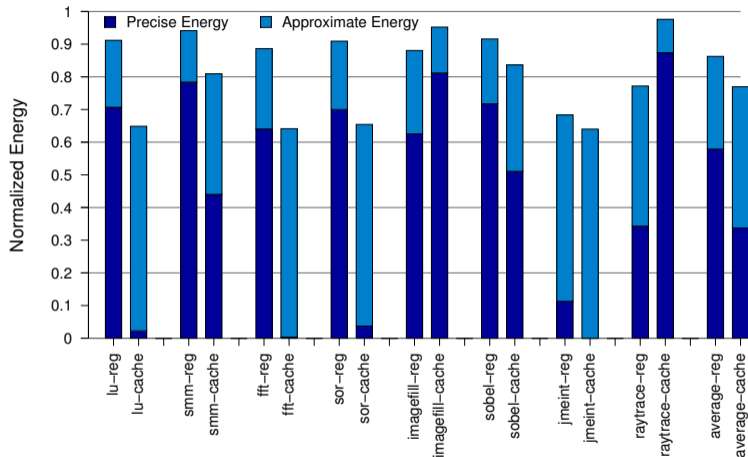
Address: 0 ... 0 1 0 0 0 1 1 0 0 0

Approx.: **0** 0 ... 0 1 0 | 0 0 1 | 1 0 0 0

Tag
Index
Line
Byte

- EnerJ
 - Implemented our own Cache Model
 - New Error Models
- Eight benchmarks
- Energy Estimation
 - Gate Equivalents
 - CACTI

Results — Energy



- 32% average energy reduction for the register file
- 36% average energy reduction for the L1 cache
- 18% average energy reduction for arithmetic

Results — L1 DC Miss Rate

Benchmark	Original (%)	Approximate (%)	Improvement (%)
lu	5.11	2.67	48%
smm	7.00	4.36	38%
fft	15.91	0.004	100%
sor	2.13	1.08	49%
imagefill	17.26	11.62	33%
sobel	0.10	0.05	50%
jmeint	1.30	0.65	50%
raytrace	0.50	0.25	50%

Summary

- We live in interesting times
 - CMOS scaling is reaching its end
 - Emerging devices have new characteristics
- Continued scaling leads to unreliable devices
 - Approximate computing
 - Trading power and performance against precision
- Multi-value devices
 - Dual-mode architecture
 - Binary format for reliable operations
 - Quaternary format for efficient operations

Thank You for Listening

