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Cross-Layer Early Reliability Evaluation for the Computing cOntinuum

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Early Component-Based System Reliability Analysis for Approximate Computing Systems

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OUTLINE

- MOTIVATIONS
- SYSTEM RELIABILITY ANALISYS
- EXPERIMENTS
- CONCLUSIOSN

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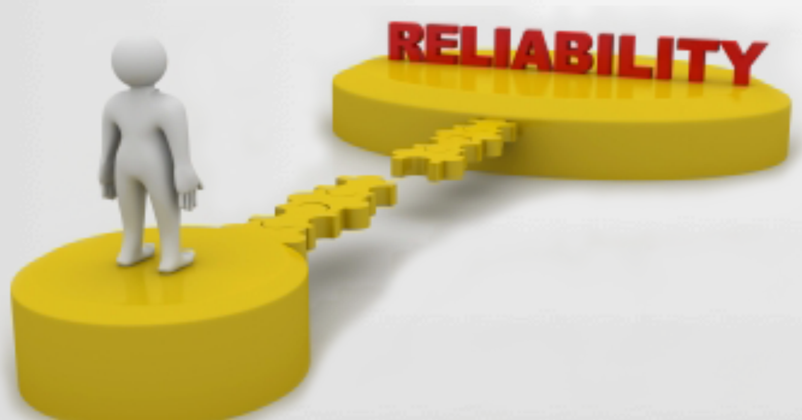
MOTIVATIONS - CROSS LAYER RELIABILITY

How do we manage reliability of digital systems today?

Error management solutions at all design layers are feasible: **technology**, **hardware**, **software**, etc.

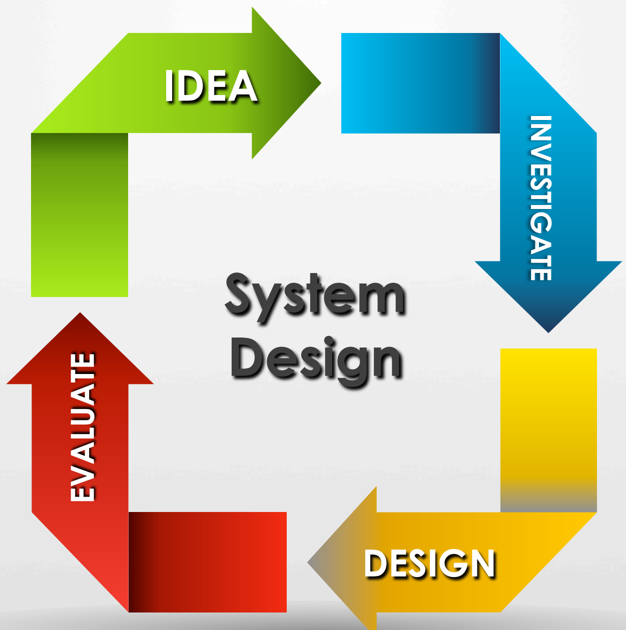
What's the best combination?

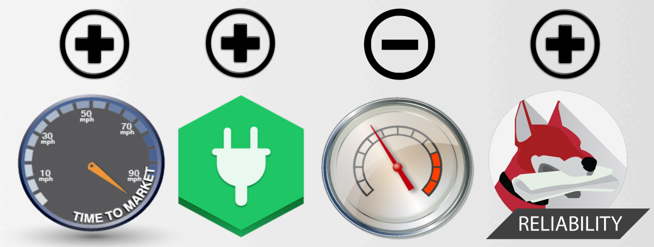


MOTIVATIONS - RELIABLE VS APPROXIMATE COMPUTING

An unsafe approach: APPROXIMATE COMP.

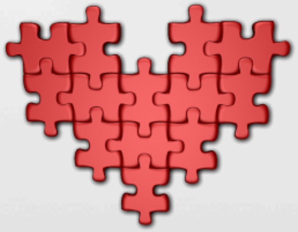
Reduced margins
Reduced redundancy





A safe approach: OVERDESIGN

Large margins
Massive redundancy



MOTIVATIONS - OBJECTIVE OF THE WORK

- How much Approximate Computing Systems can afford to reduce margins and redundancy?
  - (−) Low margins and low redundancy mean higher raw error rate
  - (+) Some applications can tolerate inaccurate results
  - (+) Errors are often masked by several layers of hardware and software

WE PROVIDE TOOLS TO EVALUATE SYSTEM RELIABILITY EARLY IN THE DESIGN CYCLE.

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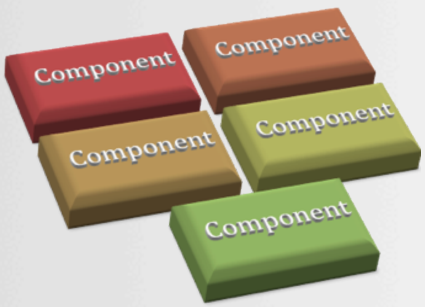
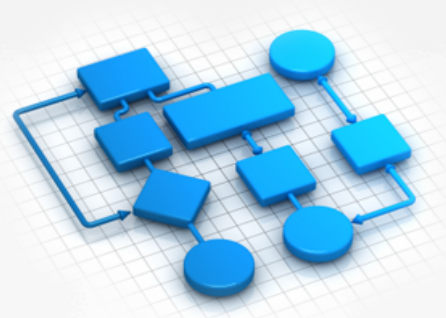
SYSTEM RELIABILITY ANALYSIS

Component-Based reliability model

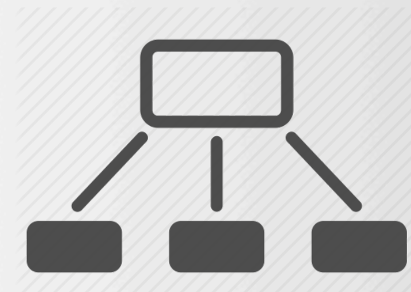


Reliability estimated using parameters of individual **components** (e.g., FIT, size, complexity, etc.)…



and their interconnections (the **system architecture**).

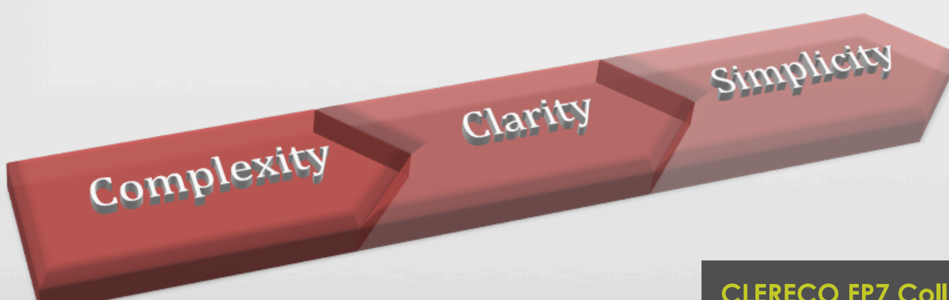
Hierarchical



Hierarchical analysis to manage complexity

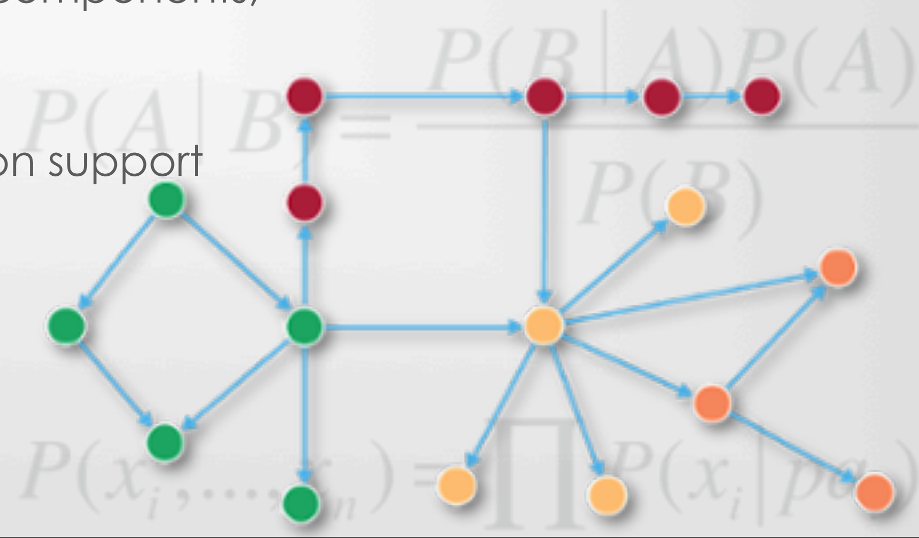
Statistical reasoning

Enable statistical reasoning on system level reliability



SYSTEM RELIABILITY ANALYSIS

- Our model exploits Bayesian Networks (BNs) as a statistical foundation for full system reliability estimation.
- Why?
  - Efficient calculation scheme,
  - Intuitive representation of all system components,
  - Capability of fitting on field data,
  - Compact representation and decision support



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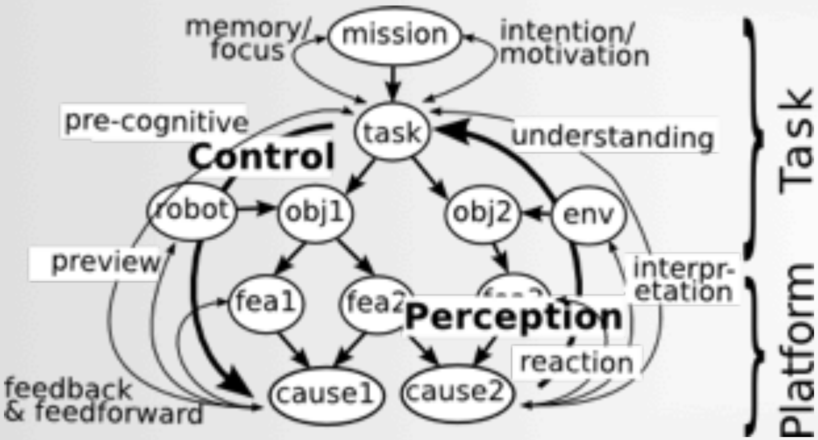
SYSTEM RELIABILITY ANALYSIS

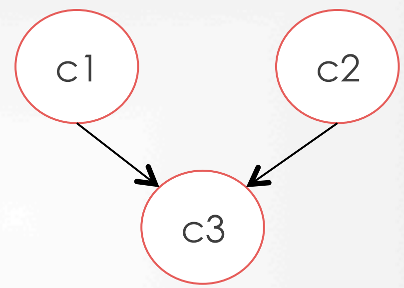
QUALITATIVE MODEL



Models the architecture of the system:

- Nodes correspond to components,
- Arcs define temporal or physical relations among components

QUANTITATIVE MODEL



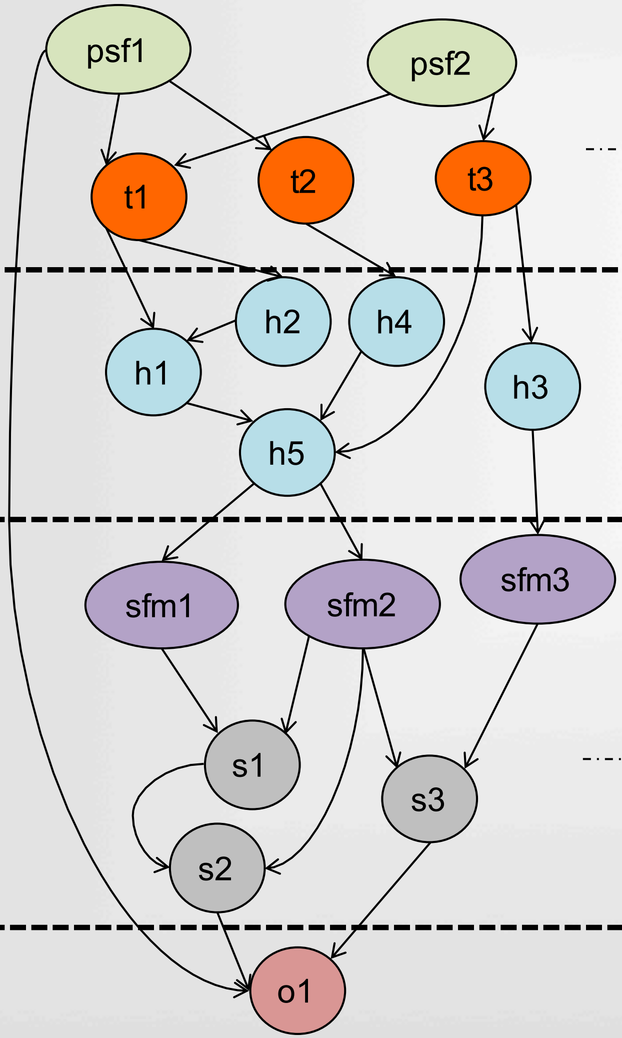
States
H: fault-free
F: faulty

P(c3=F | c1=F and c2=F)

c1	c2	c3: F	c3: H
F	F	•	
F	H		
H	F		
H	H		

Models state probabilities as a set of Conditional Probability Tables (CPT).

SYSTEM RELIABILITY ANALYSIS - QUALITATIVE MODEL



Technology domain (TD)

Physical Sources of failures
(e.g., temperature, location, voltage, etc.)

Technologies
(e.g., 18 nm bulk CMOS,14 nm Fin-FET, etc.)

Hardware domain (HwD)

(e.g., CPU, Register file, L1/L2 cache, RAM, custom IP cores)

Software domain (SwD)

Software fault models
(e.g., wrong operand, wrong instruction, control flow error, etc.)

Software modules
(e.g., custom functions, libraries, system calls, etc.)

System domain (SD)

SYSTEM RELIABILITY ANALYSIS - QUANTITATIVE MODEL

- Building the quantitative model can be both difficult and time consuming
- It is typically an assignment given to a group of specialists that need to collect information and organize them according to the model
- **We provide an ecosystem of tools able to compute CPTs for major classes of software and hardware modules**

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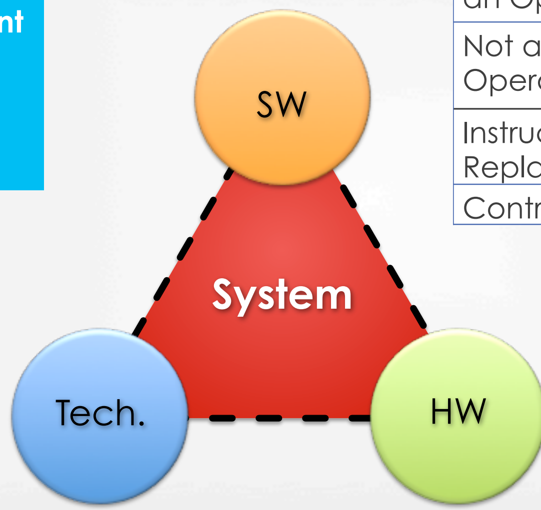
SYSTEM RELIABILITY ANALYSIS - QUANTITATIVE MODEL

LLVMFI
LLVM based fault injection model
Abstract permanent/transient fault models
Fine grained software faulty behavior classification

Software Fault Model

Fault Model	Description
Wrong Data in an Operand	An operand of the VISA instruction changes its value
Not accessible Operand	An Operand of the VISA instruction cannot change its value
Instruction Replacement	An instruction is used in place of another
Control Flow Error	The Control Flow is not respected



CPUs (GEFIN)
x86-64 OoO model
ARM OoO A9/A15 model

GPUs
NVIDIA G80, GT200 and Fermi Architectures
AMD Southern Island, Evergreen

Memories
SRAM, DRAM, Flash, STT-MRAM

Interconnections
PCI Express, AMBA, NoC

Custom cores

Technology Library
soft errors

Technology node
- Bulk Planar (ASU PTM Models) 22 nm and 16 nm
- Bulk FinFET (ASU PTM Models) 20 nm and 14 nm
- SOI Planar (UTSOI Model) 22 nm

X

Circuits
- LATCH
- SRAM Cell 6T/8T/10T
- FLIP-FLOP D
- LOGIC GATES

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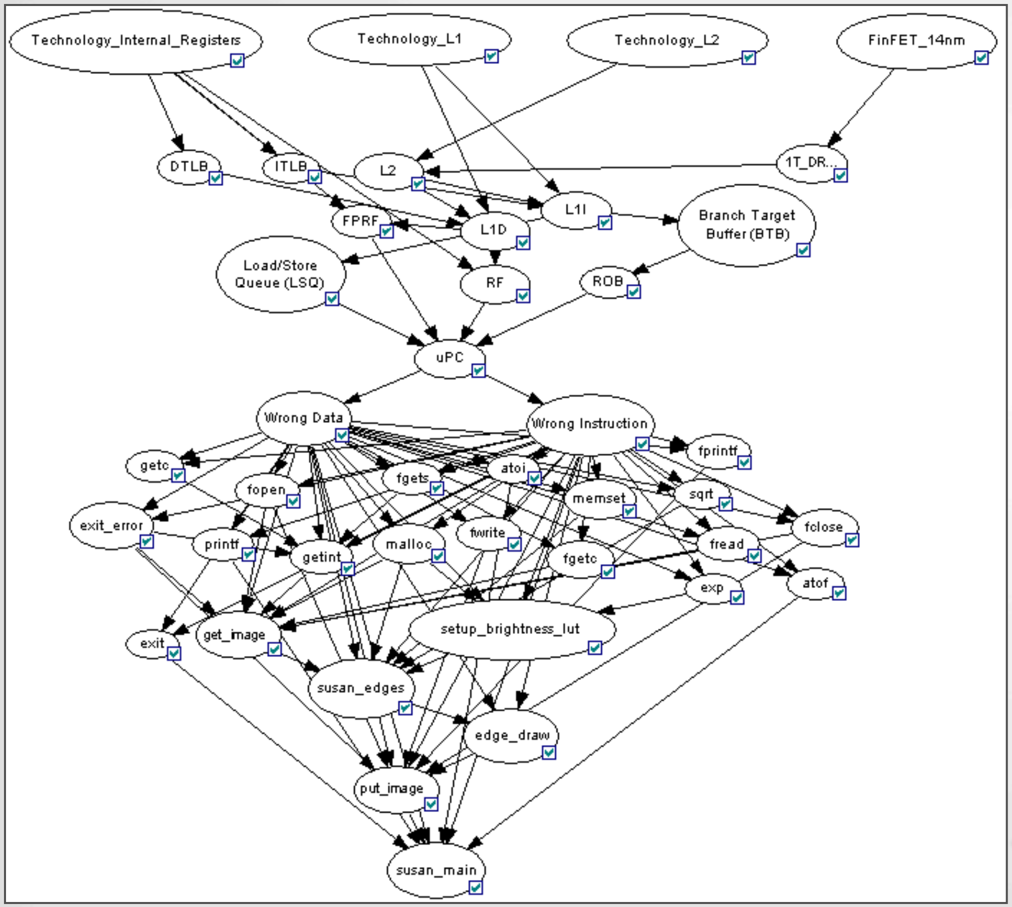
SYSTEM RELIABILITY ANALYSIS - REASONING



1 **Predictive reasoning**

Starting from information about causes (i.e., raw technology failure rates) to new beliefs about their effects (i.e., system failures), following the forward directions of the network arcs.

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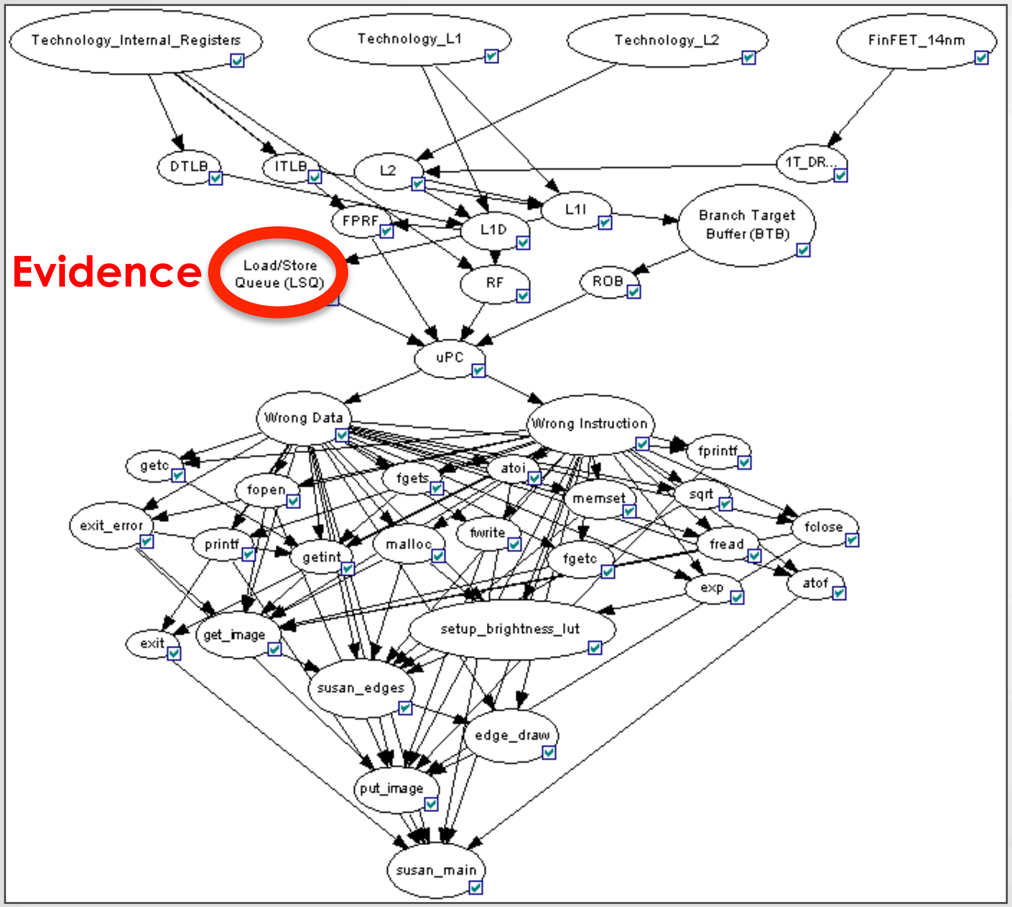
SYSTEM RELIABILITY ANALYSIS - REASONING



2 Design exploration

Starting from the evidence that a node is in a given state (i.e., failure) to new beliefs about its effect.

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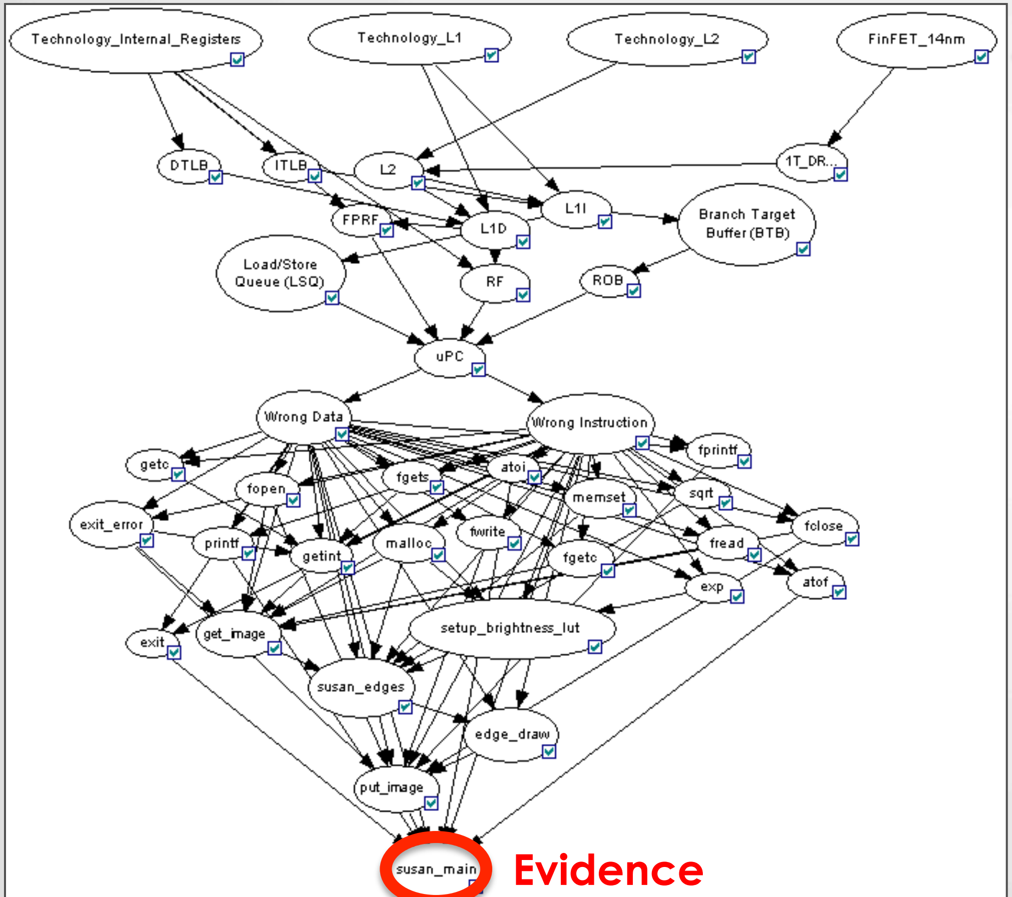
SYSTEM RELIABILITY ANALYSIS - REASONING



3 **Diagnostic reasoning**

Reasoning from symptoms to cause, such as when we observe a failure in the system, we can update our belief about the contribution of each node (hardware or software component) to this failure.

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EXPERIMENTAL SETUP

- Technology Domain:
  - 22nm Bulk Planar (FIT: 194,7E-7 single bit flip FIT rate 6T SRAM cells under typical conditions 1V, 50°C)
- Hardware Domain
  - x86 out-of-order CPU and ARM Cortex A15 out-of-order CPU
    - Register file (256 regs each 64-bits) 2KB, L1 Instruction Cache (2KB),L1 Data Cache (32 KB), L2 Cache (1MB) , Load/Store Queue (128B)
  - ECC Protected DRAM
- Software Domain
  - Linux operating system executing one of the following MiBench programs: (1) susan smooth, (2) susan edges, (3) susan corners, (4) qsort, (5) string search, (6) sha, (7) jpeg decode, (8) jpeg encode, (9) aes decode, (10) fft

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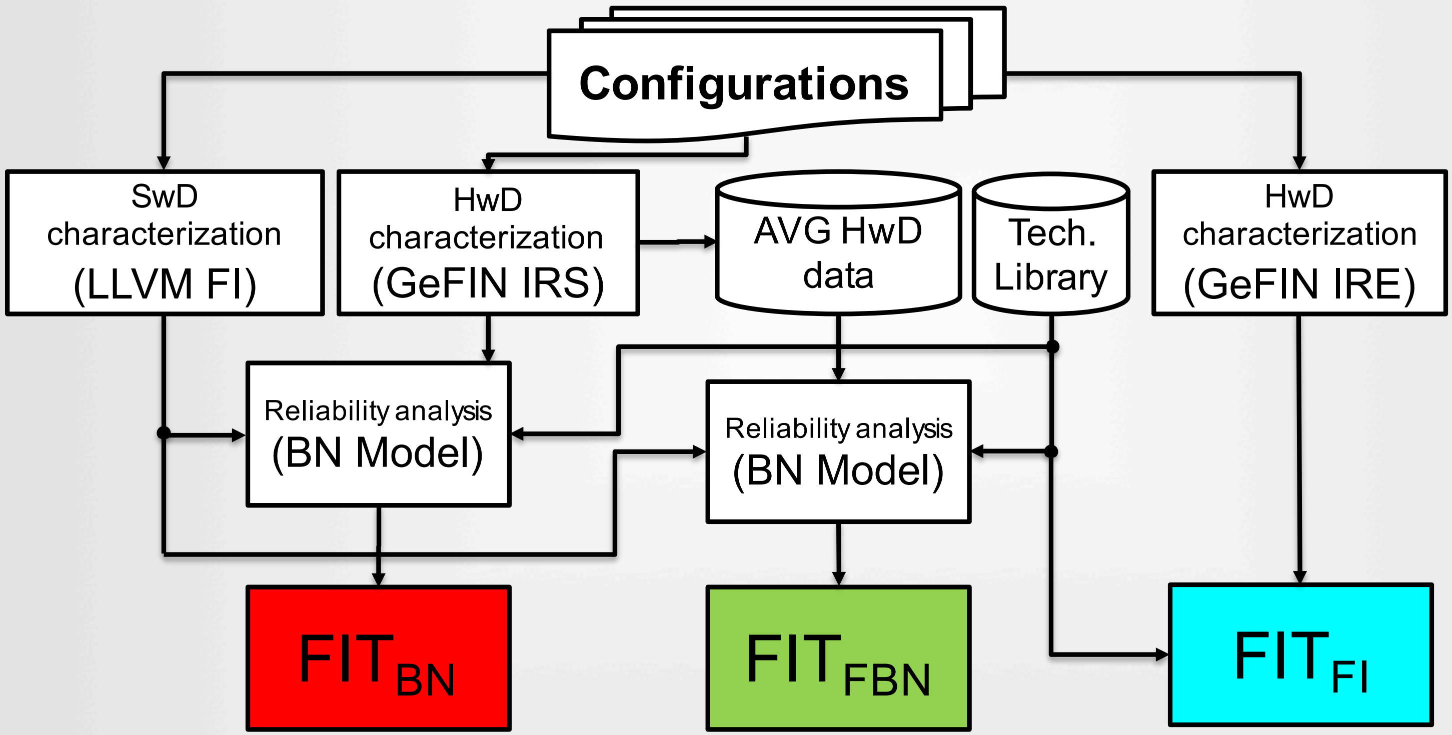
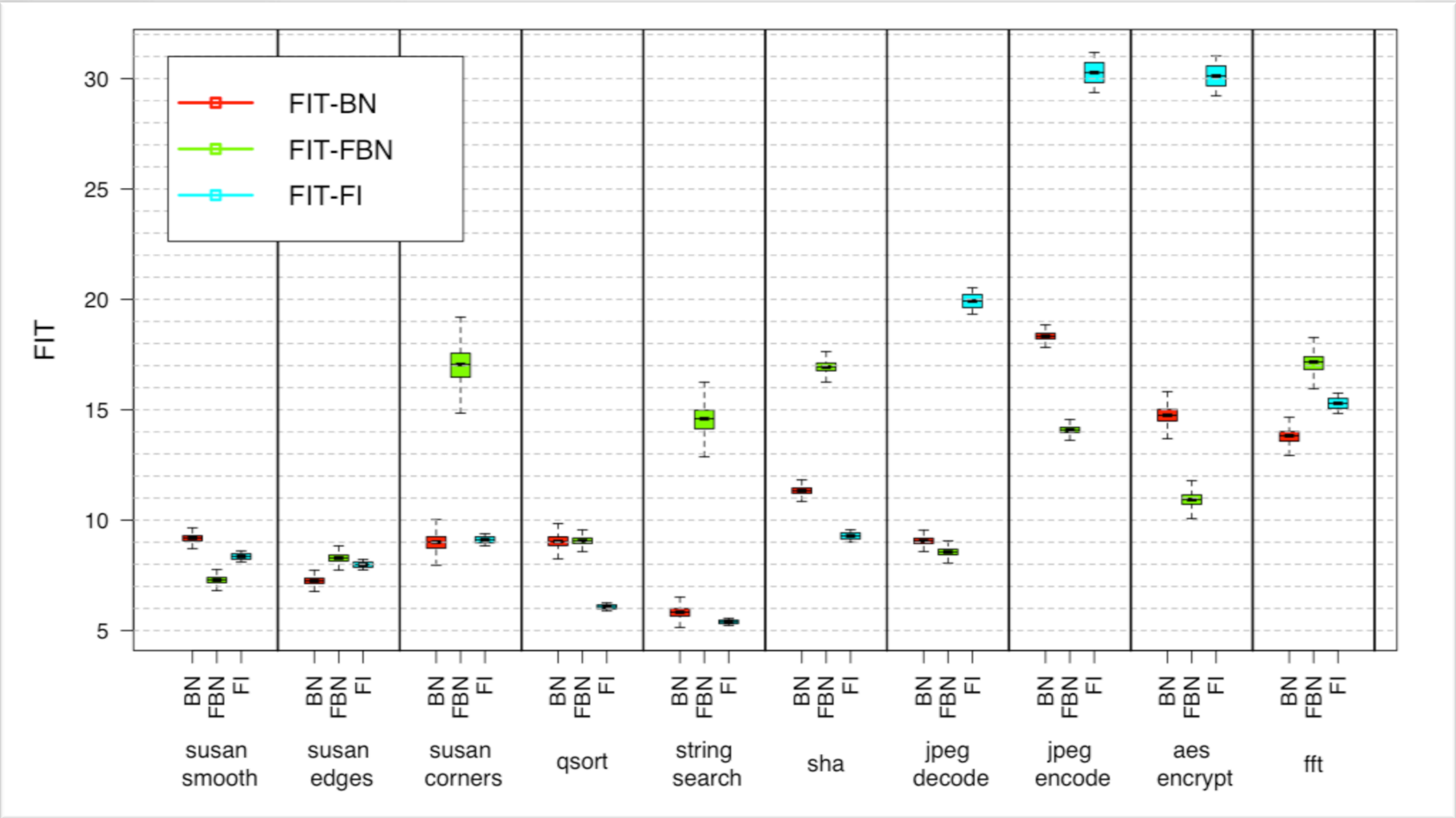
EXPERIMENTAL RESULTS - SETUP



Component characterization performed using statistical fault sampling according to [Leveugle et al. DATE 09] with 3% error margin and 99% CL.

EXPERIMENTAL RESULTS - ACCURACY



FIT estimation for the 10 selected benchmarks running on the X86 based architecture.

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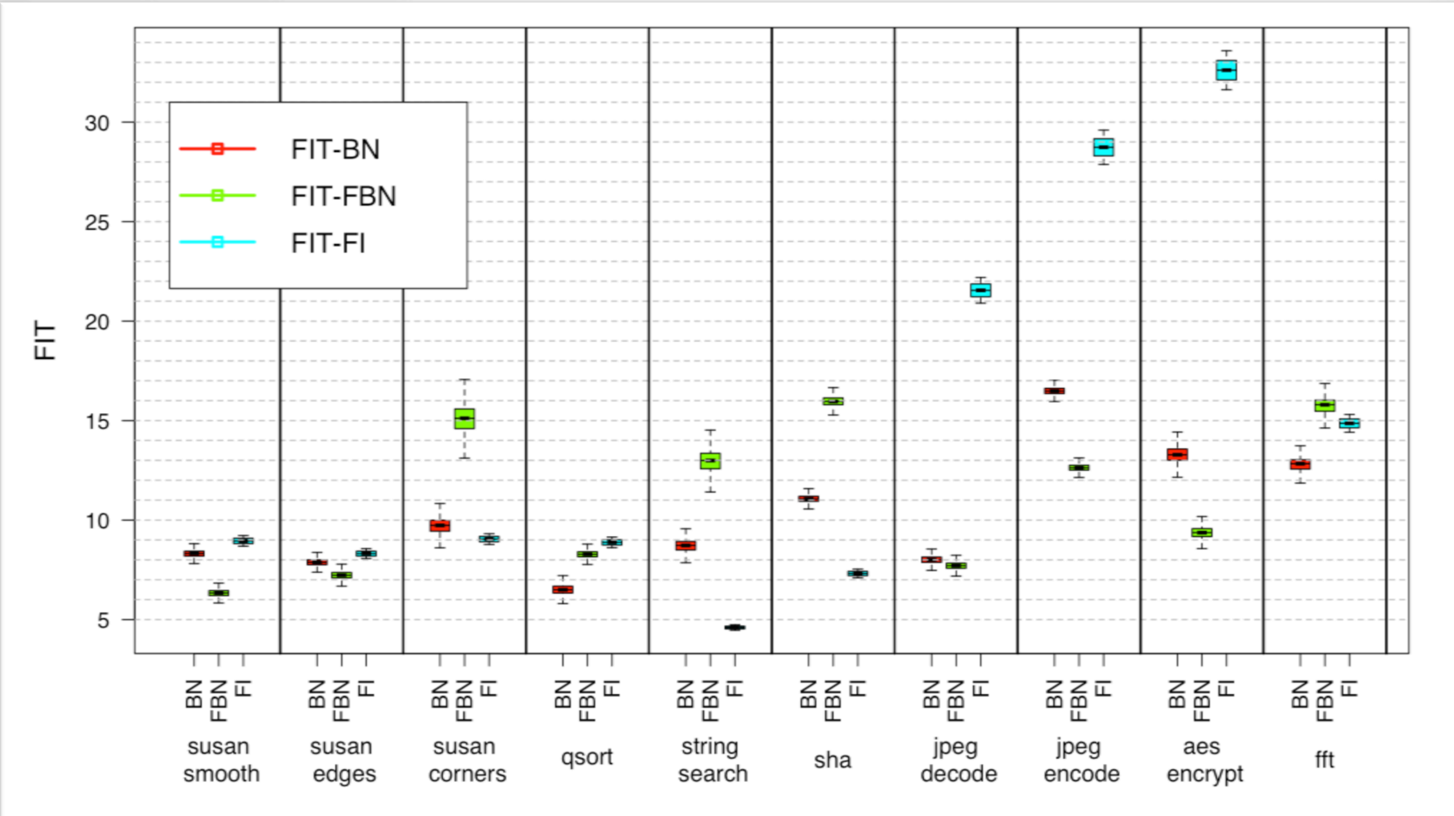
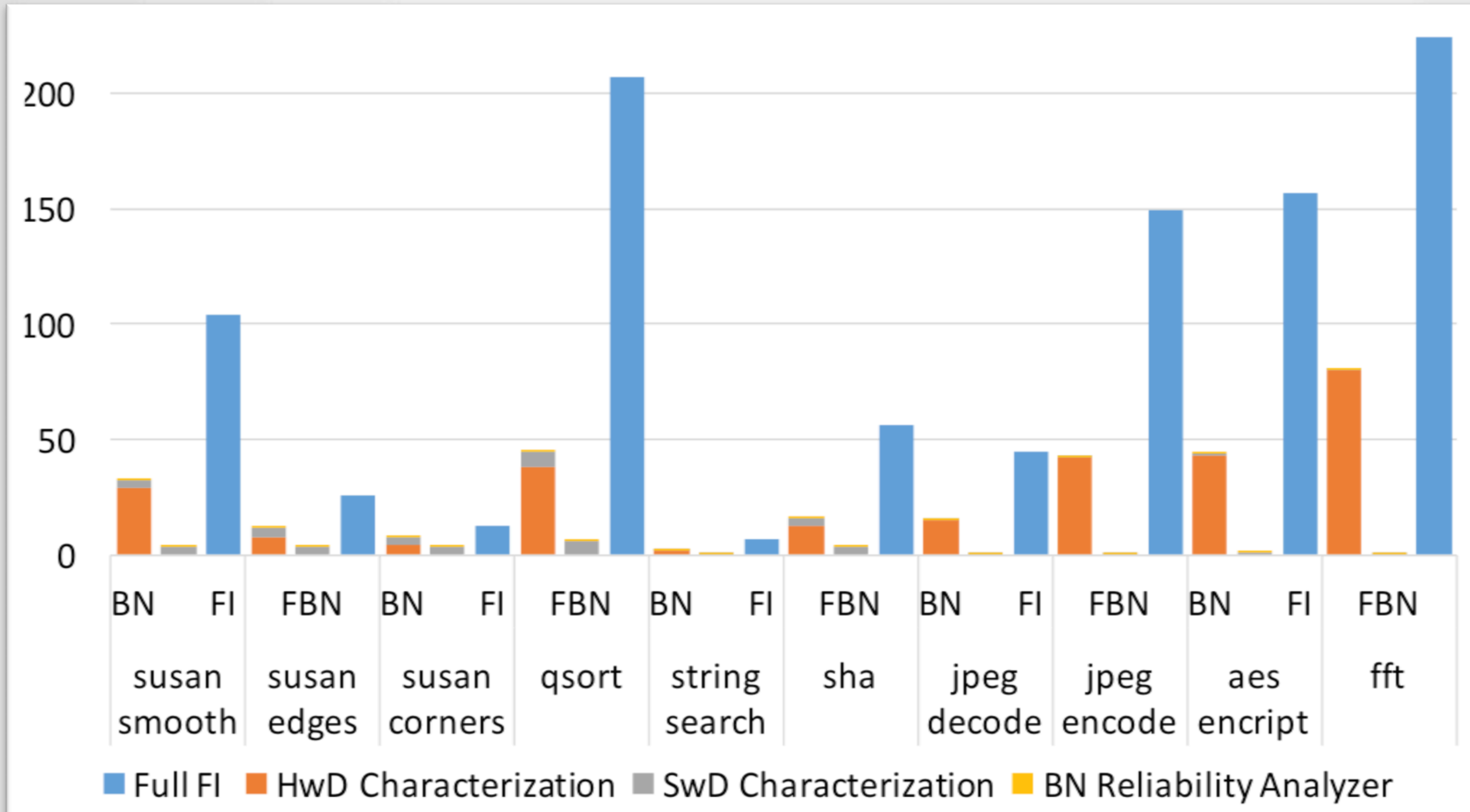
EXPERIMENTAL RESULTS - ACCURACY



FIT estimation for the 10 selected benchmarks running on the ARM A15 architecture.

EXPERIMENTAL RESULTS – SIMULATION TIME



Performance comparisons (hours of simulation).

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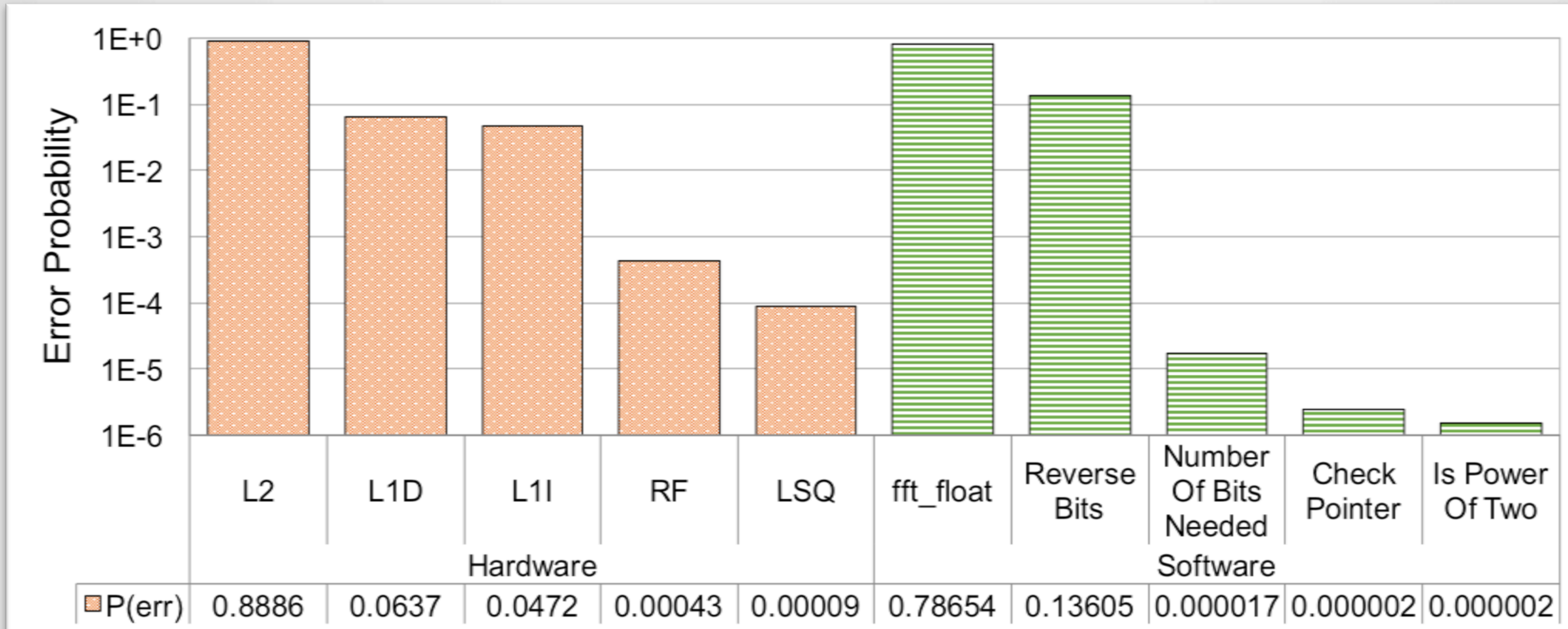
EXPERIMENTAL RESULTS – DIAGNOSTIC REASONING



Example of backward reasoning for the x86 fft configuration

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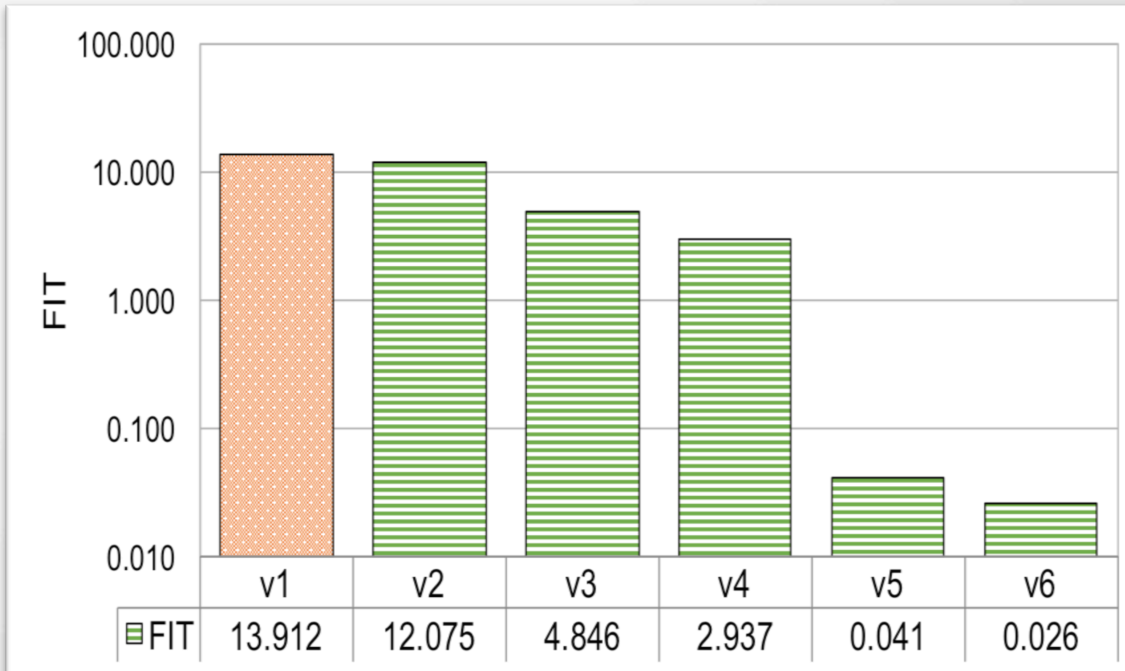
EXPERIMENTAL RESULTS – DESIGN EXPLORATION

Variant	Reverse Bits	fff_float	L2
v1	U	U	U
v2	FT	U	U
v3	U	FT	U
v4	U	U	FT
v5	U	FT	FT
v6	FT	FT	FT



Example of design exploration and optimization

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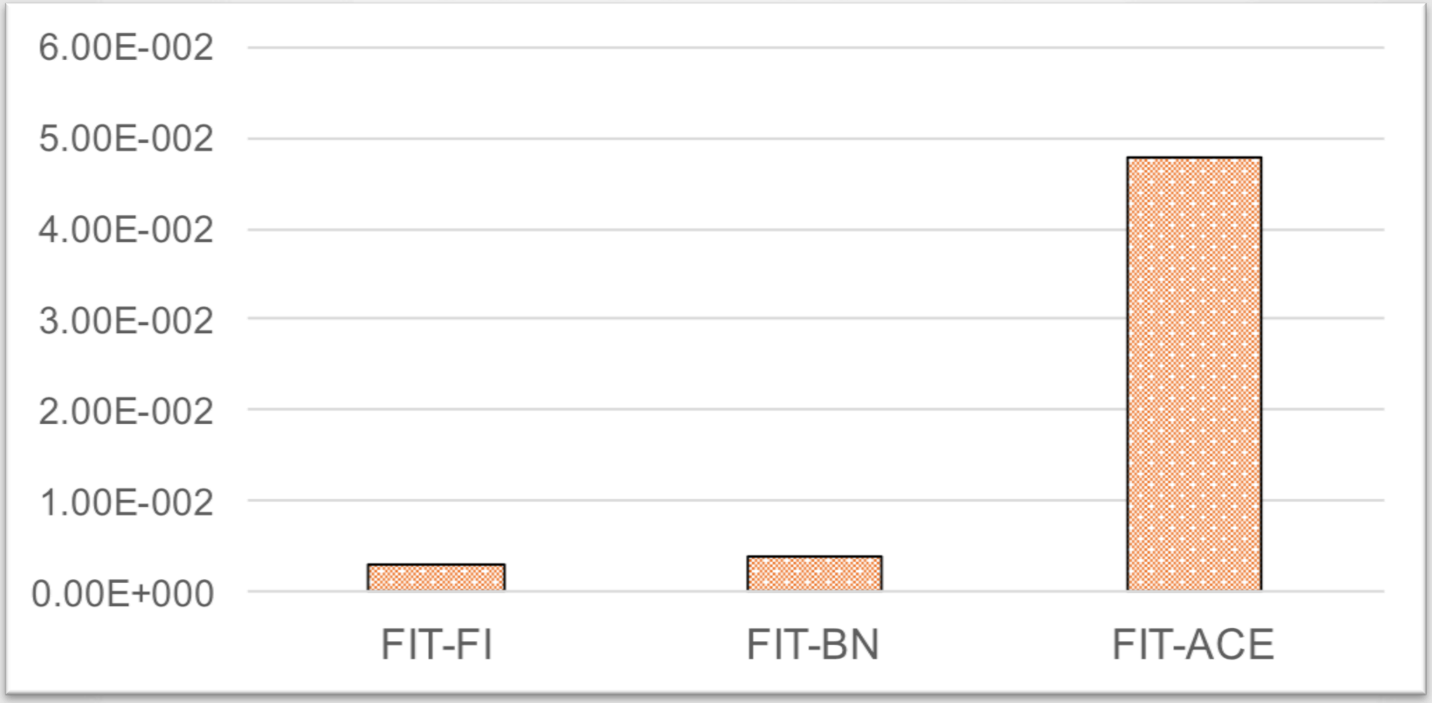
EXPERIMENTAL RESULTS – COMPARISON WITH ACE ANALISYS



Comparison with AVF computed through ACE analysis for the string search benchmark.

AVF computed based on data extrapolated from [George et. al DSN'10]

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  - TECHNOLOGY/ENVIRONMENT ANALYZER
  - HARDWARE ANALYZER
  - SOFTWARE ANALYZER
  - STATISTICAL REASONING
- EXPERIMENTS
- **CONCLUSIOSN**

CONCLUSIONS

- We presented a full framework for system level reliability analysis
  - Enables analysis early in the design cycle to enable design exploration
  - Provides a full ecosystem of tools to help designers building the reliability model
  - Provides very accurate results with reduced computation time

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mauruuru
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mochchakkeram
go raibh maith agat
sukriya
kop khun krap
sagolun
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