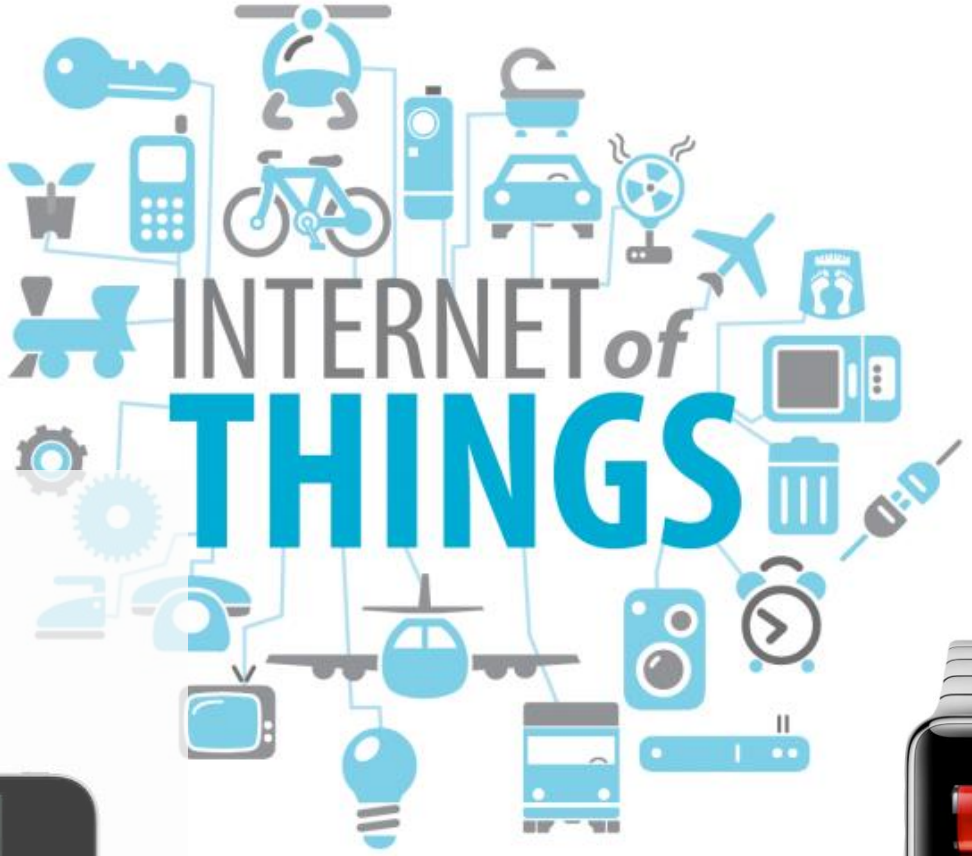
Under-limits Voltage Scaling: The benefit of Approximate Computing

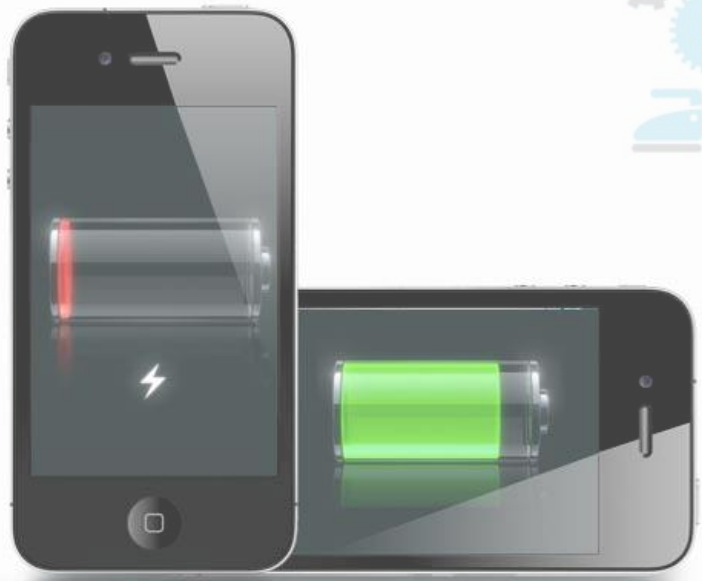
Alberto Bosio (LIRMM), Miroslav Valka (ST-TIMA)
France
bosio@lirmm.fr

Outline

- Introduction
- Proposed Approach
- Experimental Results
- Conclusions

Introduction





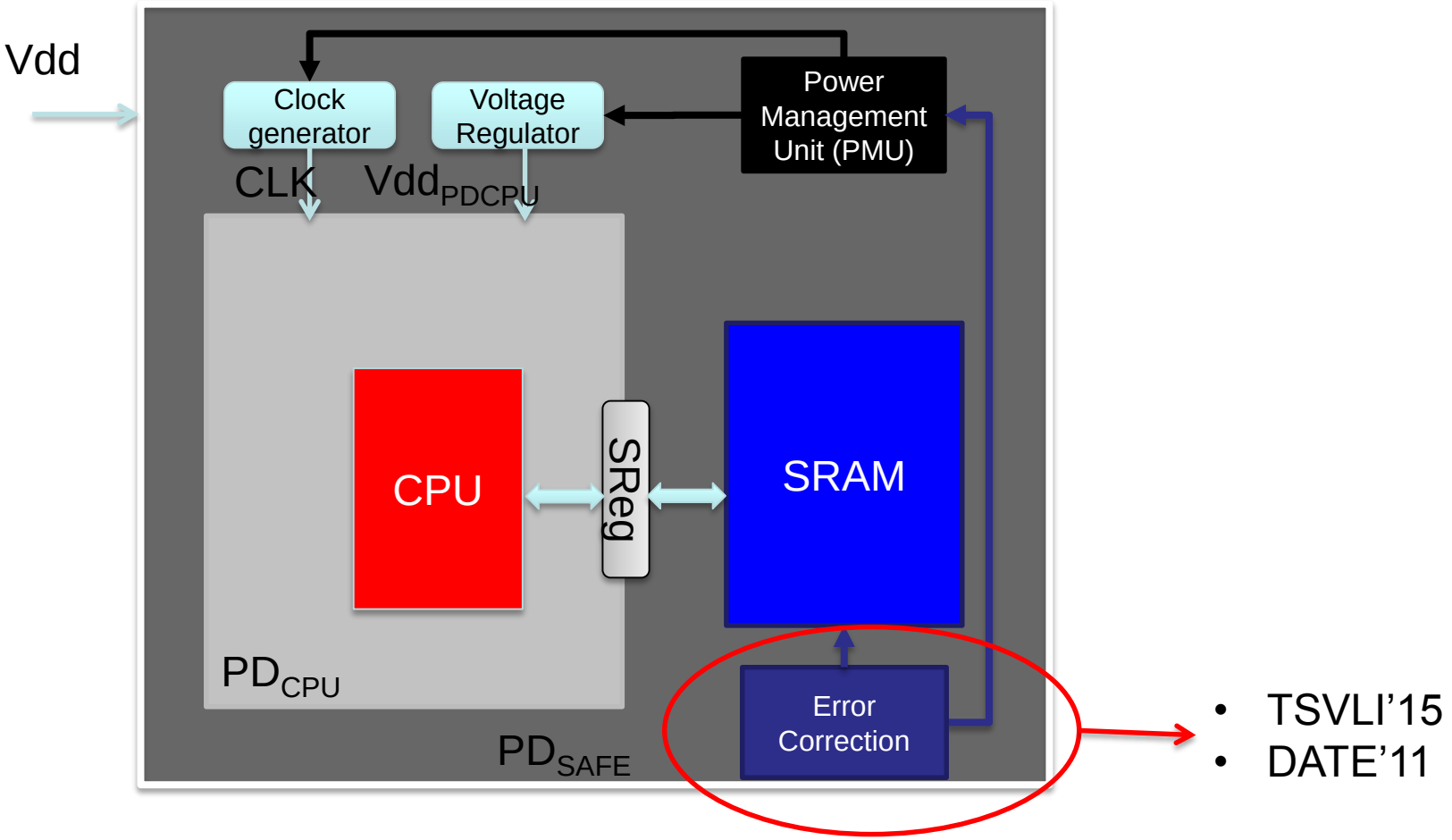
State-of-the-Art

- Approximate Computing
  - Reduces the supplied V_{dd}

- Save energy

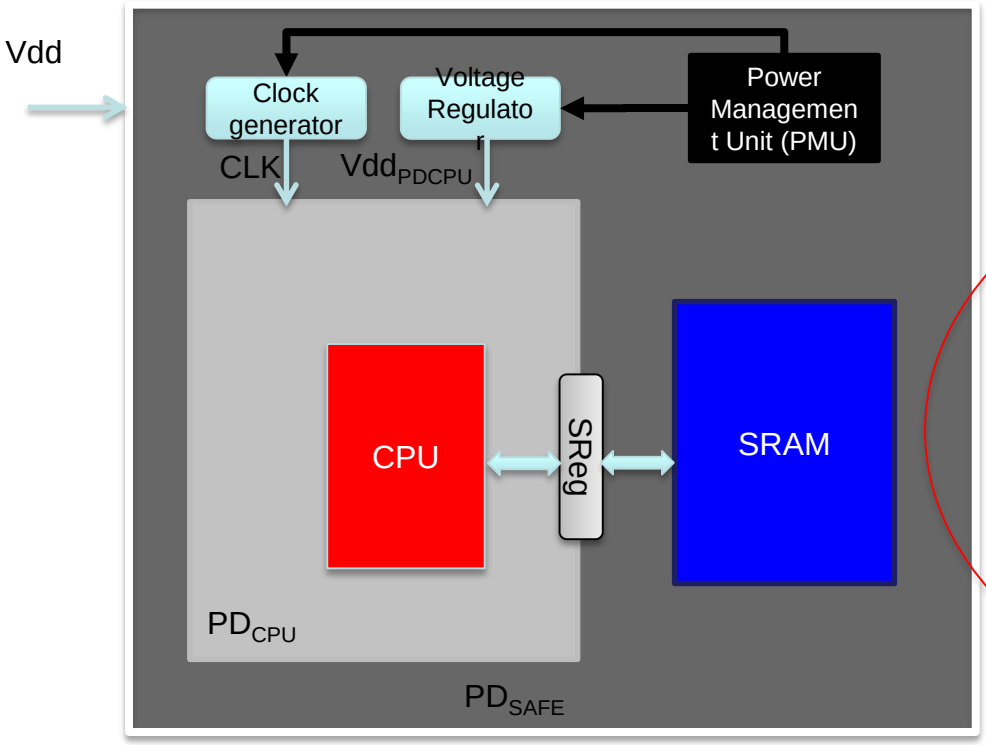
- Faults (timing errors) can appear

State-of-the-Art



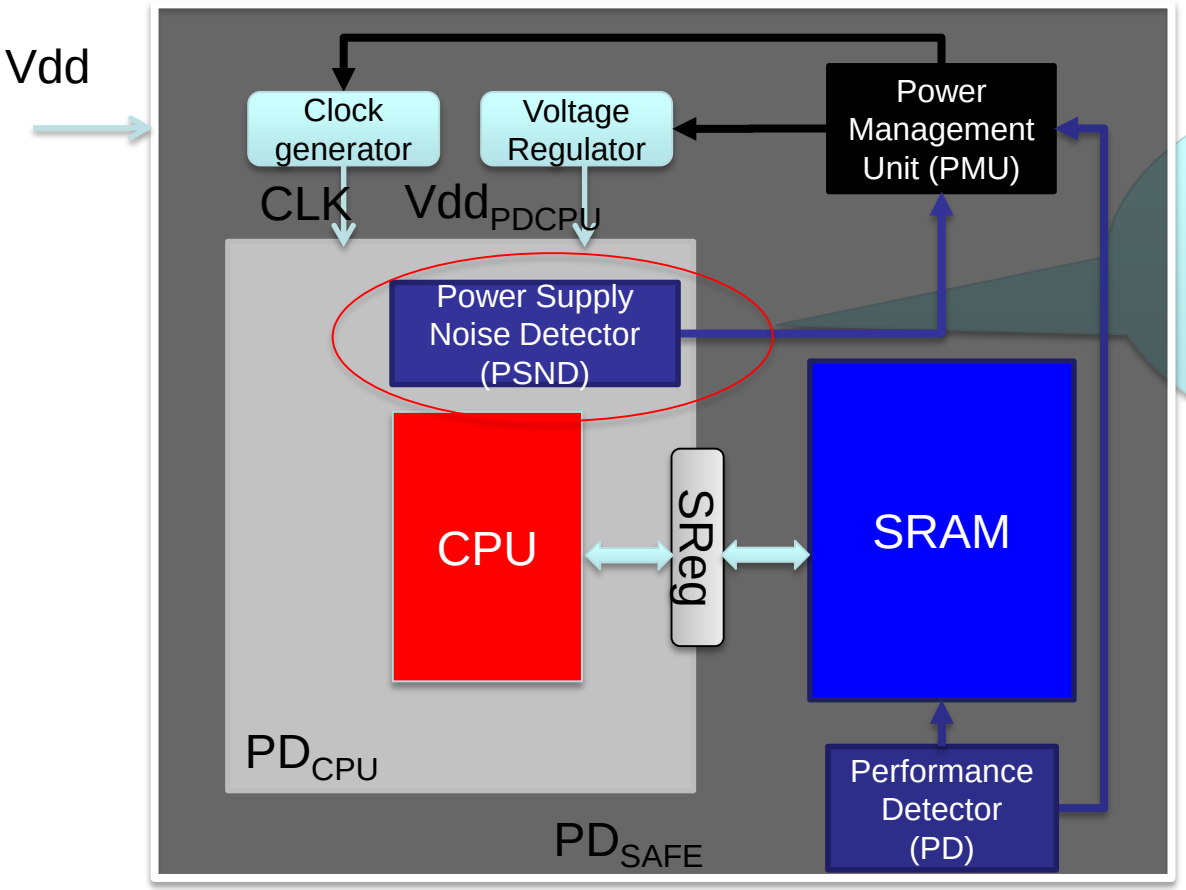
- TSVLI'15
- DATE'11

State-of-the-Art



The application can “tolerate” errors

Proposed Approach

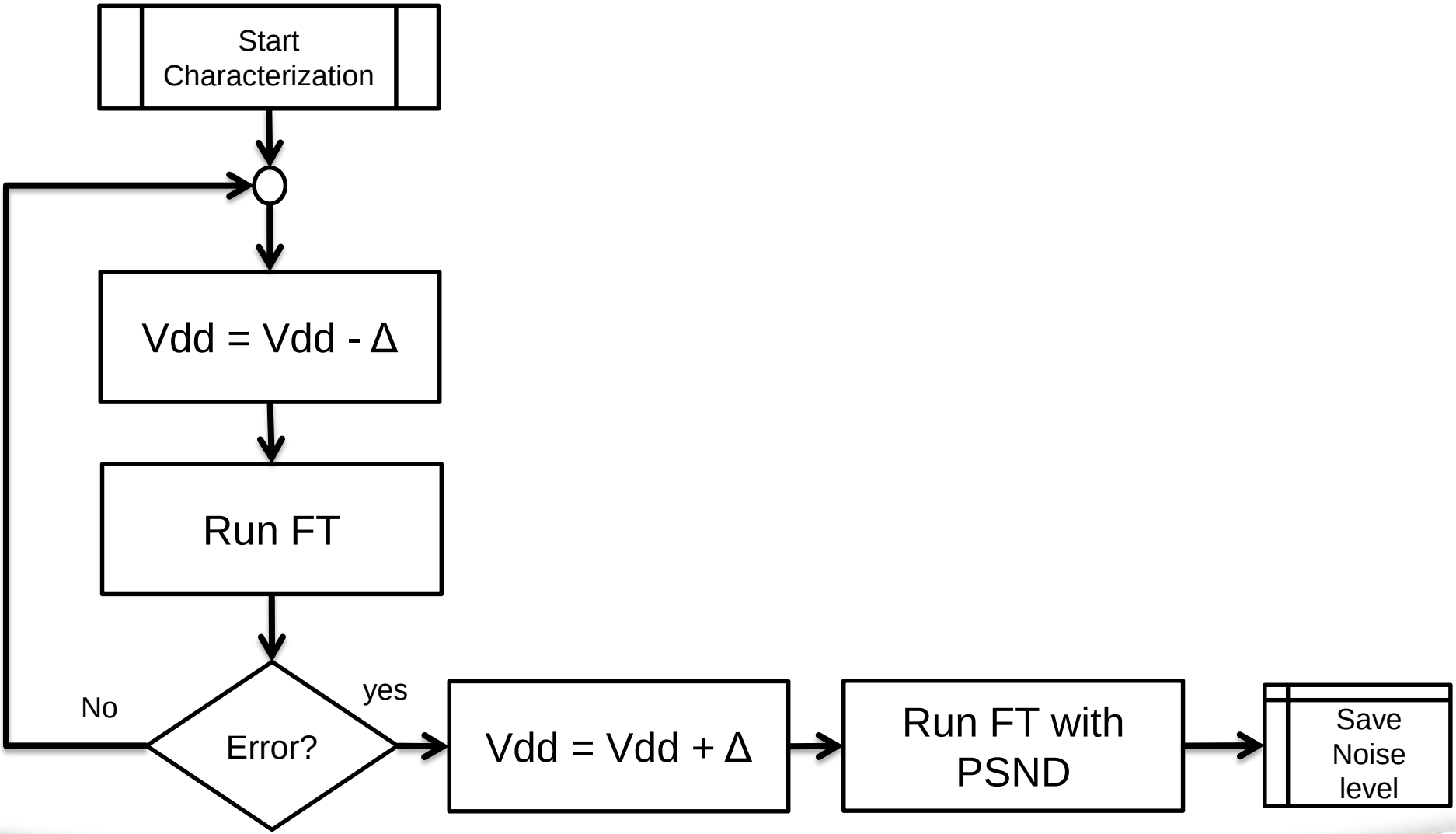


Reduces the Vdd until the "**noise**" reaches a so-called "**critical level**"

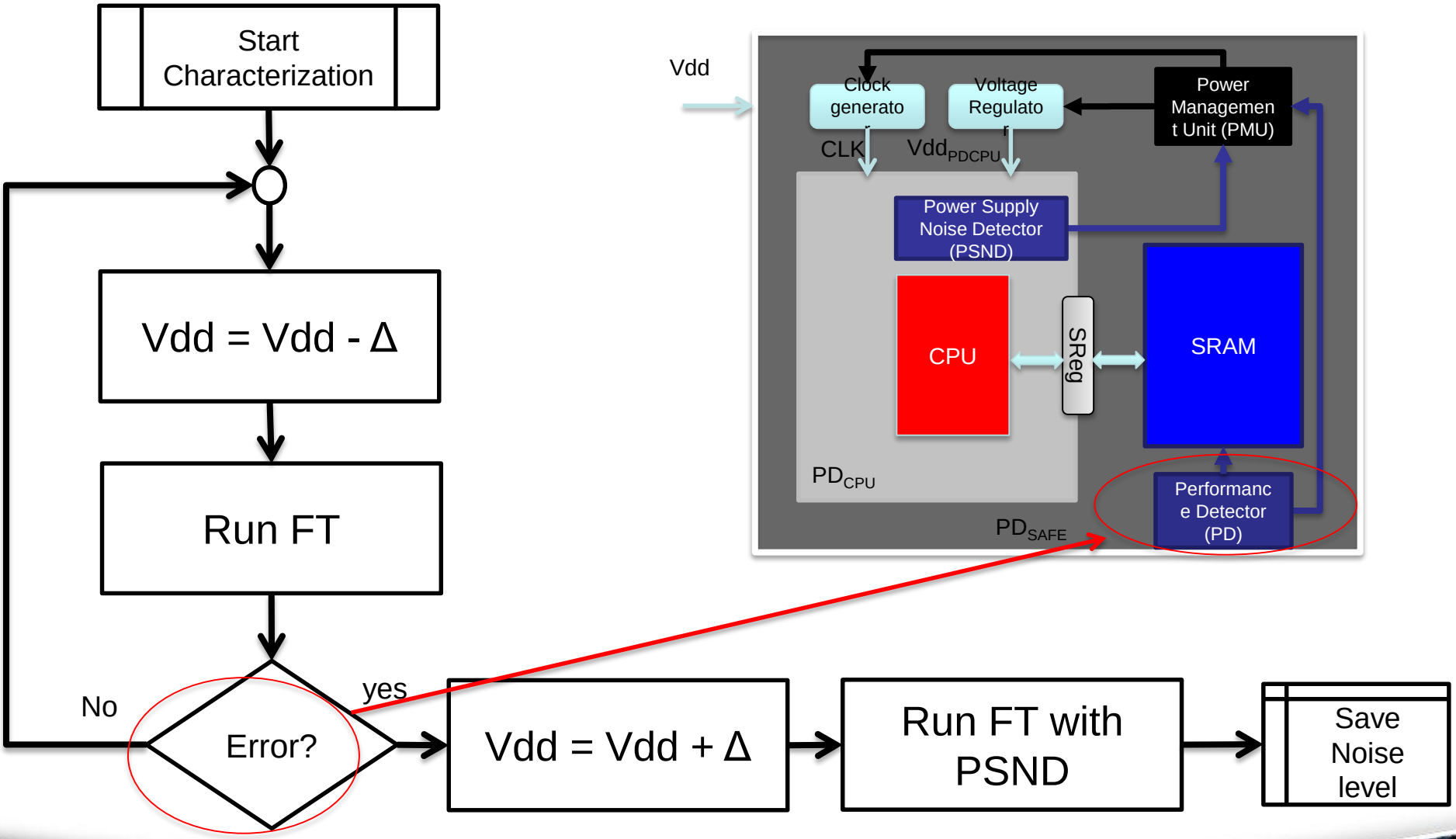
Characterization Phase

- Run a dedicated stress program called Failing Test (FT)
  - As short as possible
  - Maximize the CPU activity
- Generate by using the approach of [VLSI-SoC'11]

Characterization Phase

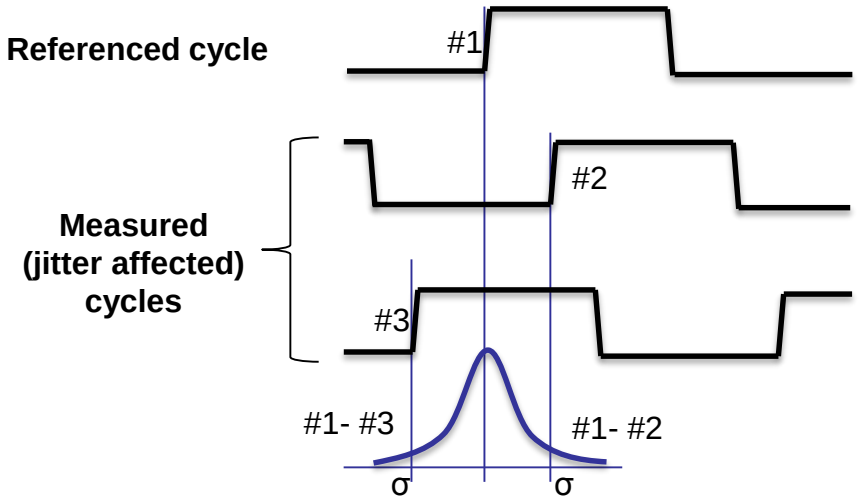


Characterization Phase

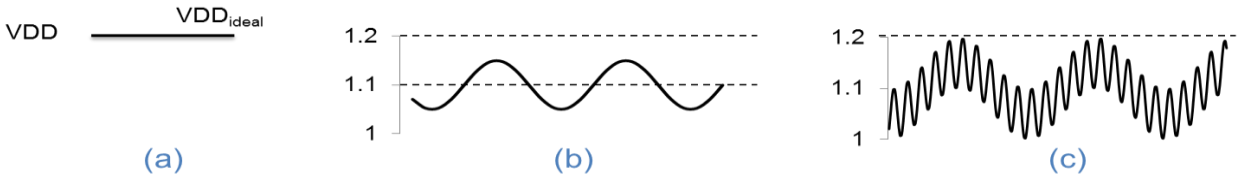


Noise Sensor

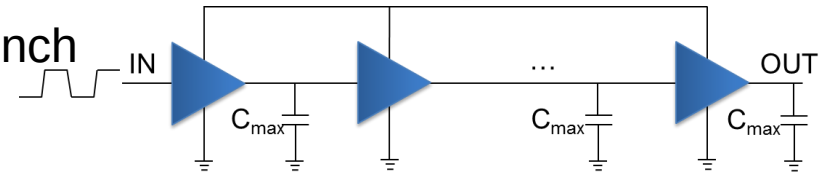
- Noise induced because the V_{dd} is too low w.r.t. the CPU activity
  - Power Supply Noise (PSN)
  - It can impacts he **jitter** of a given signal

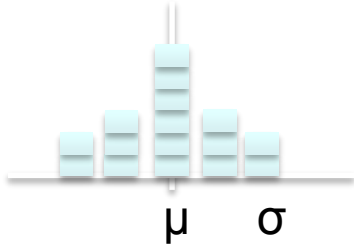


PSN affects Jitter



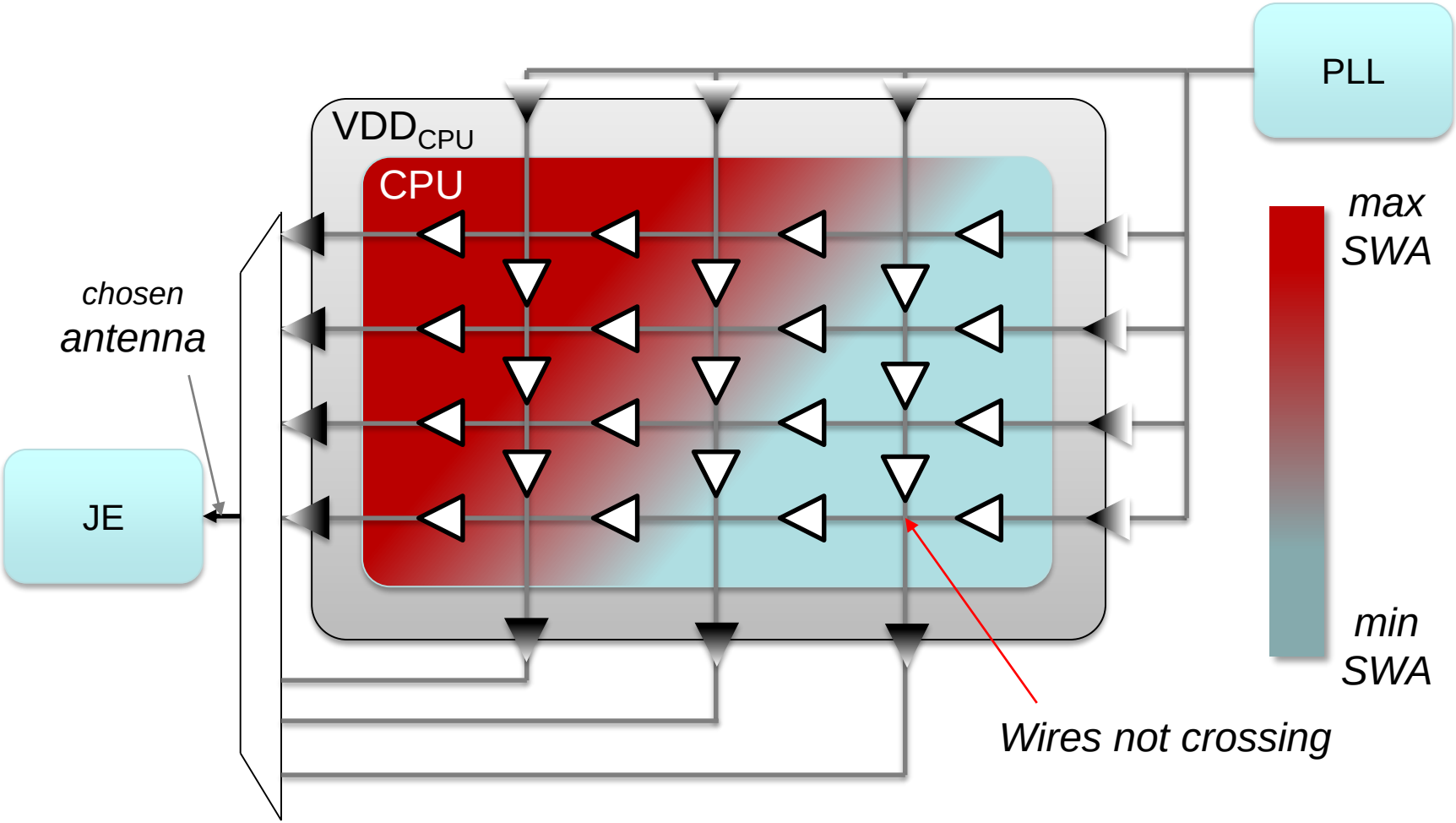
Simple Bench



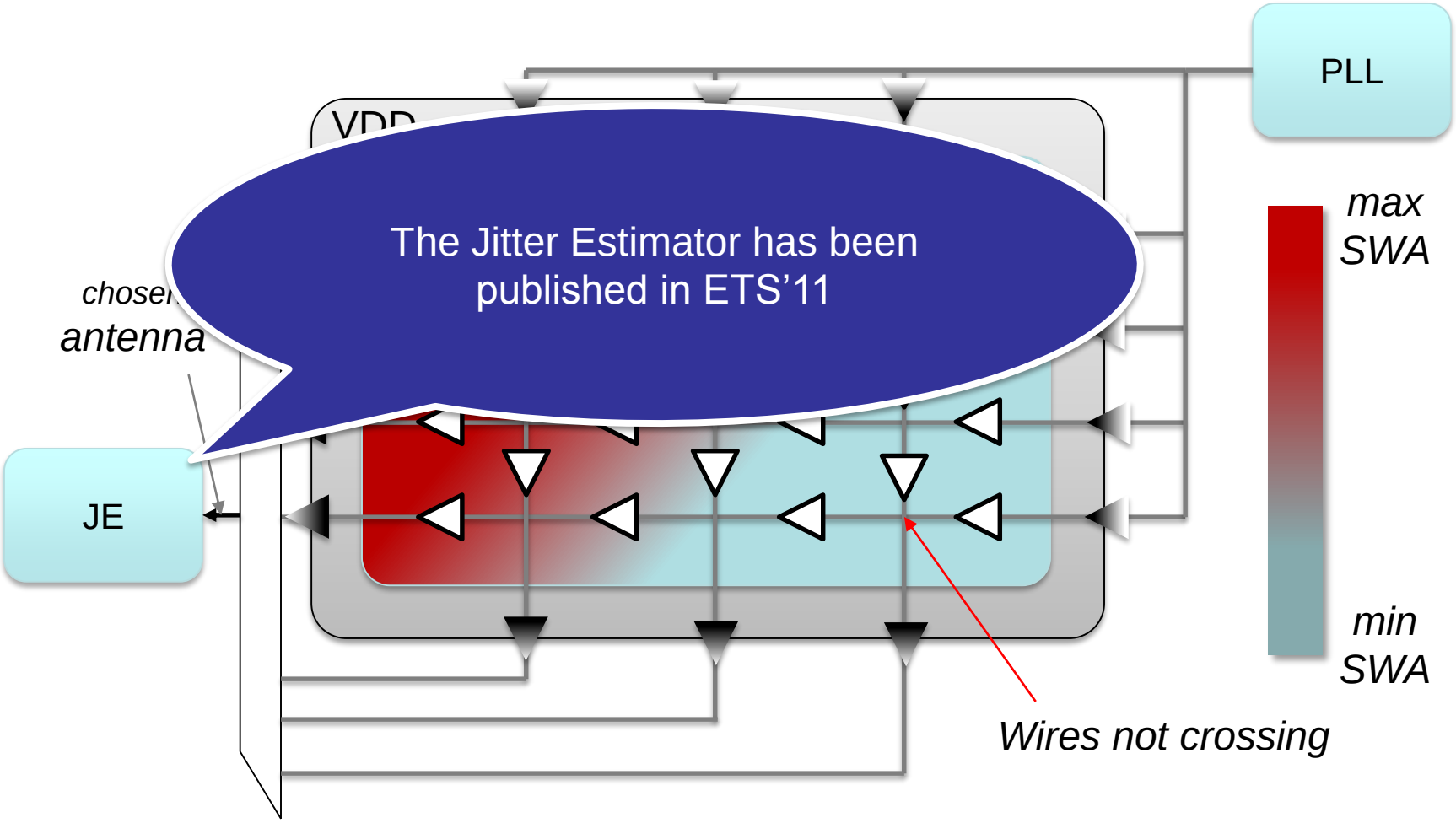


Power supplies	T_{IN}/T_{PSN}	μ value of T_{IN} on T_{out} [ps]	σ [ps]
VDD ideal	0.3	300	0
Low Freq (LF)	0.3	299	7.14
LF + High Freq	0.3	300	11.27

Selecting the Signal



Selecting the Signal



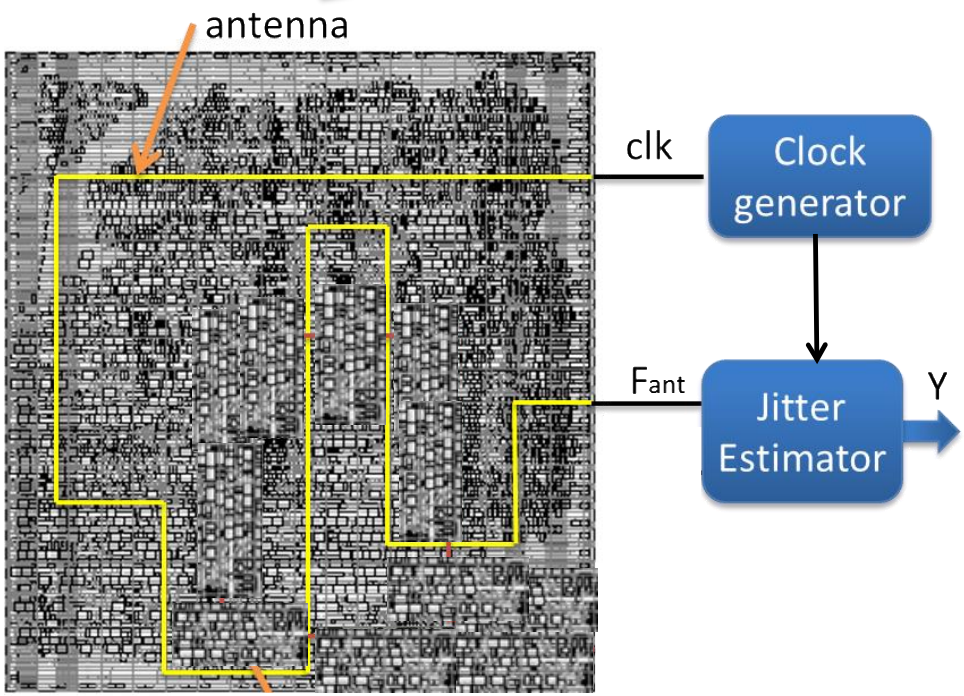
Experimental Results

- Case study:
  - CPU core : MSC-51 (mc8051)
  - memory SRAM (64k*8bit)
  - @28nm FDSOI

Vdd	1V
Vdd_{cpu}	1V
#PI	66
#PO	96
#gates	8316
# FFs	578

Experimental Results

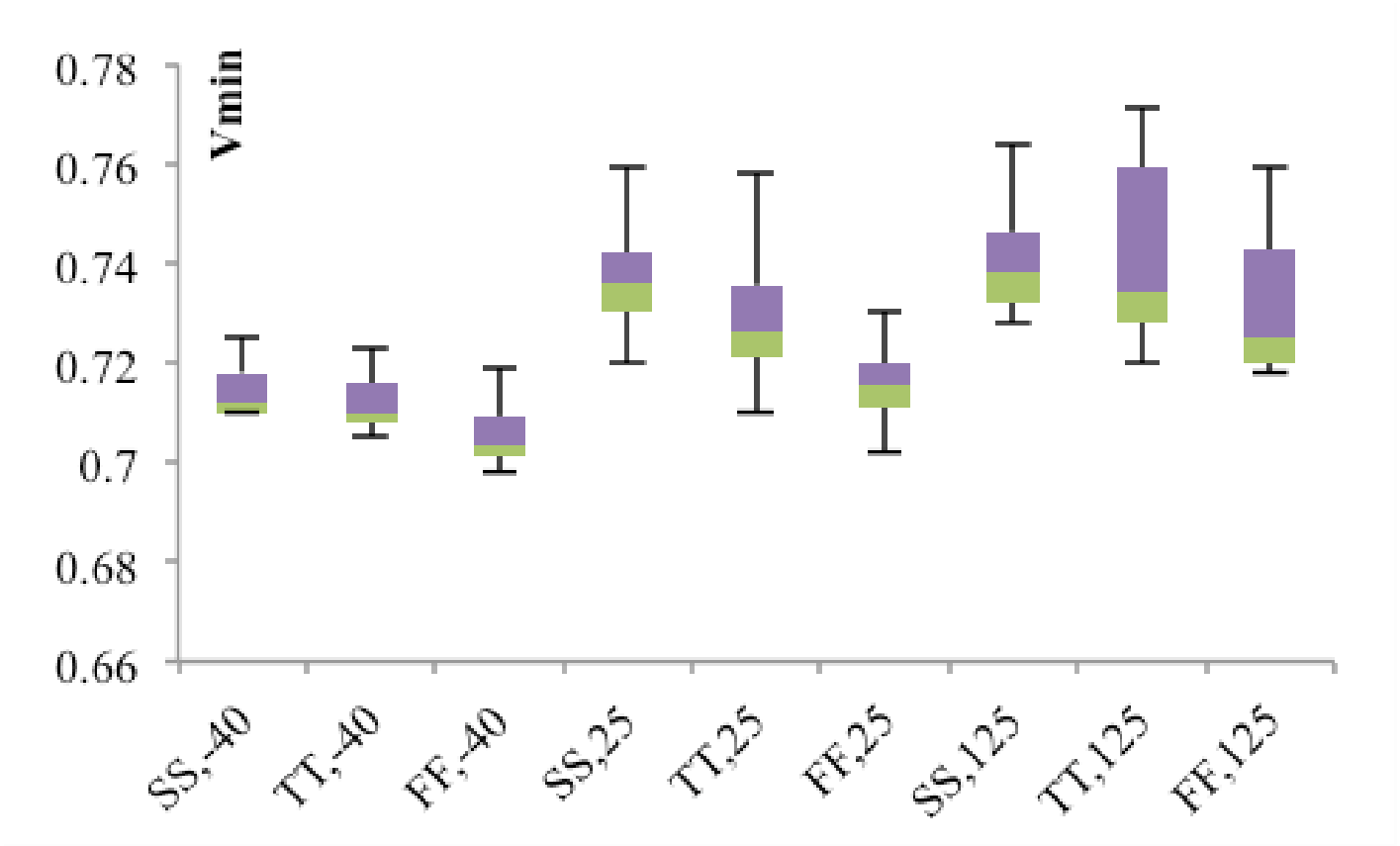
It is composed of 300 delay elements



Experimental Results

- The Failing Test has been generated by using the tool and the methodology described in [VLSI-SoC'11]
- The execution time of the FT is less than 1 second
- Characterization phase
  - It requires about 1 minute

Experimental Results



Conclusions

- Effective approach for adapting the V_{dd} depending on the running application
- Characterization phase
  - Approximate computing -> reduces V_{dd} until errors appear
- Sensitive to external conditions
- In average 25% of V_{dd} reduction

- A lot of things… It would be good if
  - We could automatically understand that the application starts to fail -> due to external conditions or aging effects
  - Re-run the characterization phase
  - Increase the operation life of the system