Genetic Improvement for Approximate Computing Position paper

Lukáš Sekanina and Zdeněk Vašíček

Brno University of Technology, Faculty of Information Technology Brno, Czech Republic sekanina@fit.vutbr.cz

IT4Innovations national018#80 supercomputing center@#01%101



HIPEAC WAPCO 2016

Introduction



- Search-based software engineering
 - applies metaheuristic search techniques to software engineering problems that can be formulated as optimization problems
- Genetic improvement (of <u>existing</u> software)
 - is the application of evolutionary and search-based optimization methods with the aim of improving functional and/or non-functional properties of existing software
- Genetic programming (GP)
 - one of evolutionary computing methods capable of automated creation of software

Genetic improvement of software





Bowtie2, a widely-used DNA sequencing system, consisting of 50k lines of C++ code, was reduced by GI to 20k lines of code; with an average 70 times faster execution than the original code

Langdon and Harman: IEEE Tr. On Evol. Computing. 19(1), 2015

Other examples

- T FIT
- automatic bug fixing (real bugs in real C programs)
 - W. Weimer, et al. Automatic program repair with evolutionary computation. Communications of the ACM, vol. 53, no. 5, pp. 109–116, 2010.
- an improved version of C++ code from multiple versions of a program written by different domain experts (e.g. improved MiniSAT)
 - J. Petke, et al. Using genetic improvement and code transplants to specialise a C++ program to a problem class. In 17th European Conference on Genetic Programming, LNCS, vol. 8599. Springer, 2014, pp. 137–149

• improved CUDA programs (DNA analysis SW)

• W. Langdon. Improving CUDA DNA Analysis Software with Genetic Programming. In Genetic and Evolutionary Computation Conference (GECCO 2015): 1063-1070 Observation: The Genetic Improvement method has not accepted solutions increasing the error (w.r.t the original implementation) Let us use Genetic Improvement and tolerate some errors!



The median function



corrupted image (10% pixels, impulse noise)

filtered image (9-input median filter)



Median as a comparator network





Approximations conducted by means of genetic programming



FIT

Impl	Time $[\mu s]$				Energy [nWs]		
Impi.	STM32	PIC24	PIC16		STM32	PIC24	PIC16
6-ops	2.8	54.5	170.5		86	377	342
10-ops	3.3	70.8	251.5		102	490	504
14-ops	3.9	86.8	336.5		118	600	674
18-ops	4.5	104.5	424.1		138	723	850
22-ops	5.0	116.7	487.8		151	808	978
26 - ops	5.9	130.0	558.0		179	900	1118
30-ops	6.0	142.0	627.4		181	983	1257
$34\text{-}\mathrm{ops}$	6.4	154.0	819.7		196	1066	1643
38-ops	6.9	165.5	885.0		210	1145	1774
qsort	28.5	1106.2			869	7655	—

34.9% error prob.,max. error dist. 252% power reduction

4.8% error prob., max. error dist. 1 21% power reduction

fully-working median

ops = operations in the source code.

```
#define PIX_SORT(a,b) {
    if ((a)>(b))
        PIX_SWAP((a),(b));
}
```



V. Mrazek, Z. Vasicek and L. Sekanina. GECCO GI Workshop, 2015

Conclusions



- Genetic improvement can (relatively) easily be adopted to approximate software/hardware components.
- Advantages
 - an automated method
 - Interesting solutions typically hidden to conventional methods can be discovered.
 - A multi-objective GP provides a Pareto front showing various non-dominating trade-offs.
- Disadvantages
 - time consuming process of evolution
 - non-deterministic method
 - difficult interpretation of results

DTIS 2016: Special session on Approximate Computing

- 11th International Conference on Design & Technology of Integrated Systems in Nanoscale Era
- Conference: April 12 14, 2016 in Istanbul, Turkey
- Deadline for submissions: January 27, 2016
- http://www.dtis2016.teiath.gr/



11th International Conference on Design & Technology of Integrated Systems in Nanoscale Era April 12-14, 2016, Istanbul, Turkey

Aim of the Conference: to cope with the rapidly progressing technology which, today, reaches the nanometer scale. The areas of interest include the design, test and technology of electronic products, ranging from integrated circuit modules and printed circuit boards to full systems and microsystems, as well as the methodologies and tools used in the design, verification and validation of such products. Topics of the conference include, but are not limited to:

ntegrated Systems	Integrated Systems		
Design:	Technology:		
SOC, SIP design	 Nanoelectronics 		

- Multiprocessor systems
- Embedded systems
- Wireless systems
- Network on Chip
- Analog, Mixed Signal and RF systems
- MEMS and MOEMS

Integrated Systems Testing:

Defect and fault modeling

- Nanoelectronics
- Device modeling Material
- characterization
- Failure analysis
- New components
- Packaging

- Process technology Reliability issues
- Analog and Mixed Signal testing MEMS/MOEMS testing
 - SOC and SIP testing
 - Delay testing
 - Memory testing
 - Fault Simulation, ATPG
 - DFT, BIST and BISR
 - On-line testing and fault tolerant

D	TTS	Tm	Fo
	113		10

- o Contact
- o Sponsors
- o Call for Papers

NEWS

- o 11/24/2015 Paper Submission Started
- o 01/17/2016: Deadline for Paper Submission has been extended to January 20, 2016

Thank you for your attention!

Lukáš Sekanina and Zdeněk Vašíček

Brno University of Technology, Faculty of Information Technology Brno, Czech Republic sekanina@fit.vutbr.cz

IT4Innovations national018#80 supercomputing center@#01%101

